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# SEVENTH QUARTERLY REPORT
# COMPATIBLE TECHNIQUES
# FOR
# INTEGRATED CIRCUITRY

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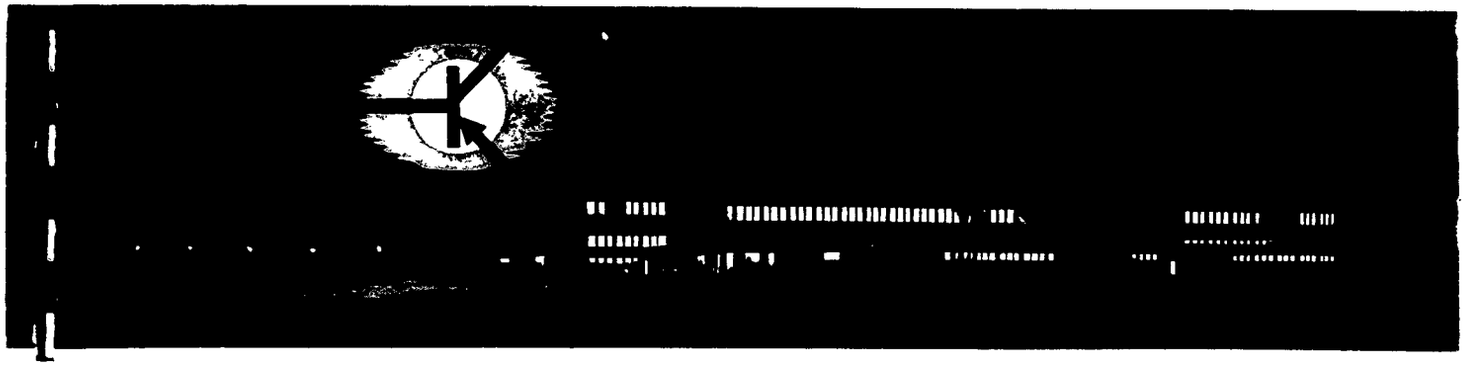

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5005 EAST McDOWELL ROAD PHOENIX, ARIZONA A SUBSIDIARY OF MOTOROLA INC.

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# 1.0 THIN FILM TECHNOLOGY

## 1.1 Status Report of Compatible Techniques for Integrated Circuits

### 1.1.1 Introduction

The objective of this program is to develop compatible techniques for the fabrication of complete integrated circuit functions through the utilization of semiconductor, thin film and other solid state technologies as required. The desired result is the successful integration of thin film and semiconductor techniques to produce useful circuit functions which are inherently reliable and reproducible.

The impetus behind this effort is the design and manufacturing flexibility to be attained through the combination of semiconductor and thin film technologies. The utilization of a wide variety of materials to construct circuit elements provides wider range of component values to closer tolerances than can be achieved if only one technology and material is used. Furthermore, the component parasitic parameters such as temperature coefficients, voltage sensitivity and loss factors can be better controlled if more than one material is available to construct components. Of great importance is the electrical isolation of critical circuit elements which is achievable when thin film elements are combined with silicon elements.

In summary, the principle advantages of a compatible thin film - single block silicon technology are listed.

1. Improved design flexibility with resultant improved function performance due to:
   a. A broad range of component values
   b. Closer tolerances of component values
   c. A wider range of component parasitic parameters such as temperature coefficients, loss factors and voltage and current sensitivities
   d. Improved electrical isolation between components
2. The possibility of improved reliability by providing a more appropriate circuit function.
3. The possibility of reduced manufacturing cost due to improved design flexibility.

### 1.1.2 Compatible Problem Areas

One of the requirements in establishing compatibility between two technologies is to first establish the material and process steps in each technology which must be maintained and which are, therefore, inflexible. The initial phase of this program was, therefore, devoted to this study with emphasis on the development of reliable and reproducible methods for producing semiconductor components by epitaxial and diffusion methods. Some of the major material and processing requirements determined which must be satisfied, lie in the areas of:

1. Proper sequences for chemical and temperature processes

2. The long term chemical and metallurgical stability of different materials in intimate contact

The following is a partial list of some of the bounds placed upon the material selection and processing which have been identified to date:

1. The initial substrate material shall be silicon
2. The final functions shall be capable of being stored for long periods at 300°C without degradation
3. Diffusion temperatures are near 1000°C +
4. Silicon dioxide can be thermally formed at 900°C
5. To provide organic free contact areas, the semiconductor block must be heated in oxygen to 500°C
6. After metalization of contact areas, the block shall not be subjected to temperatures exceeding 500°C
7. Due to migration, diffusion and alloying problems, the use of gold shall be avoided
8. Due to its electrical conductivity and excellent adherence to metals and glass, aluminum metal is to be used for interconnection
9. The minimum sealing temperature shall be 440°C for 15 minutes
10. The use of physical masks for the delineation of thin film components shall be avoided.

Paralleling the effort to determine the semiconductor processing techniques which result in reliable functions at a high yield, a second effort was carried out to determine the bounds on the materials and processing for constructing reliable thin-film components. As knowledge was generated on the processing parameters required for the silicon technology effort was made to modify the material and processing parameters of the thin film components to assure compatibility.

Thin film components and processes which have received attention are:

Resistor Films (relatively low temperature coefficients, absence of reverse leakage parasite, reduced distributed capacitance)

- Tin Oxide films for large valued resistors (gas plating)
- Nichrome films for moderate to low valued resistors (vacuum evaporation)

Dielectric Films (for capacitors which provide low loss, voltage stable, isolated devices)

- Alumina silicate glass (gas plating)
- SiO (vacuum evaporation)
- Tantalum Oxide (vacuum evaporation and wet chemistry)
- Alumina (gas plating)

Conductor Films (for metalizing around corners and also for interconnection patterns on ceramic or plastic for interconnecting functional electronic blocks)

- Aluminum (gas plating)

Reduction of Pin Holes in Thermally Grown $SiO_2$

- Alumina-silica glass (gas plating)

Some of the compatibility problems which have been solved or are under study are:

1. Tin oxide provides high valued resistors which can be readily etched to fine patterns using KMER. It makes stable electrical contact to silicon, however, at elevated temperatures it reacts with aluminum to form an insulating aluminum oxide interface resulting in an open contact. It has been determined that a film of nickel of approximately 1000 Å thick provides a satisfactory stable interface between tin oxide and aluminum.

Solutions of tin chloride sprayed upon the substrate are hydrolized at 520°C to form tin oxide films. These are doped by traces of antimony during deposition. Difficulties are encountered in control of the aging characteristic of the films and in a somewhat elevated temperature coefficient for the high ohms per square films. Effort is being devoted to the development of a 300 - 350°C deposition process which utilizes phosphorus, silicon or aluminum as a dopant. The resultant films promise to possess lower temperature coefficients for a given sheet resistance than do films deposited by the older process. Furthermore, it is believed that improved aging characteristics can be achieved and better control obtained over film properties than is available with the higher temperature process.

2. Nichrome films possess excellent long term aging characteristics as well as low and reproducible temperature coefficients. These are evaporated onto substrates maintained at a temperature of 300°C. Nichrome films make and maintain good electrical contact to silicon as well as aluminum and possess

excellent adherence to $SiO_2$. In order to manufacture fine line (.001 inch) resistors to close tolerance, methods are currently being developed to accurately etch nichrome patterns using photo resist techniques.

3. Motorola has developed a method for depositing a stable mixed oxide glass system of about 10 per cent aluminum oxide and 90 per cent silicon dioxide. The mixed glass system has a higher dielectric strength and volume resistivity than either thermally grown or reactively sputtered quartz films. The deposition method employs gas plating techniques at atmospheric pressure. The films have proved useful as capacitor dielectrics, encapsulants and as an overcoat for thermally grown $SiO_2$ to assure pin hole free insulation between film components and the silicon substrate. The glass is stable with aluminum, however, it has been somewhat difficult to reproduce. Recently, work directed towards improvement of the reproducibility of the process involving the use of new starting chemicals has provided the desired results. The newly modified process also provides films which are less strained than those previously obtained.

4. When windows are etched into substrate glass overcoats to enable electrical contact to the substrate it has been determined that a mode of failure and a reduction in yield can result. This occurs if the window sides are tapered in a manner to cause shadowing during a following process of vacuum metalizing with aluminum. Such shadowing results in either a highly thin portion of the metalizing film or in a complete open circuit.

Under development is a compatible process of aluminizing which does not require a vacuum process eliminating possibilities

of shadowing. The process utilizes pyrolysis of the liquid diisobutyl aluminum hydride sprayed onto a substrate held at 260°C. The liquid wets onto the substrate, flowing around corners and into crevices prior to pyrolysis, thus eliminating shadowing effects.

Similar organo-aluminum compounds are being investigated which pyrolize at even lower temperatures for the depositing of user conductors for multilayered printed wiring interconnect boards.

The general approach for aluminum metalizing is also under investigation for aluminizing metal leads for sono-bonding of aluminum wires.

5. Tantalum oxide dielectric capacitors are attractive due to a high dielectric constant of 26 with reasonable dielectric strength and stability. Capacitors utilizing this dielectric material possess a voltage-capacitance product of 2.5 microfarad volts per square centimeter when rated at one-fourth breakdown potential. Films are formed by vacuum evaporation of tantalum followed by an electro-chemical process which converts the outer layer of tantalum to tantalum oxide. The capacitor is completed by the evaporation of a second conducting film which forms the second electrode. Problems associated with pin holes in the tantalum are avoided by electro-chemically removing the tantalum metal behind a pin hole by a reverse-etch process prior to the addition of the second electrode.

Effort devoted to reducing the dissipation factor of such capacitors at moderate frequency due to the series resistance of the somewhat resistive tantalum electrode has been successful. An aluminum film is deposited onto the substrate just prior to the evaporation of the tantalum film. The highly conducting aluminum provides the desired low sheet resistivity for the tantalum electrode.

Problems being worked on to provide compatibility with silicon substrates are:

1. Development of the second electrode which is stable with the oxide dielectric and aluminum metal.
2. Development of a technique to provide a low resistance contact to the tantalum and aluminum electrode after anodization.

## 1.2 Compatible Thin Film Techniques

### 1.2.1 Introduction

During this period the last major problems in fabricating compatible integrated circuits using nichrome or tin oxide resistors and $SiO_2$ capacitors were resolved. Problems in providing the "coupling capacitor function" still exist..

For practical circuit design, a ratio of CAB/CBC (see Figure 1) of 100 or more is desired.

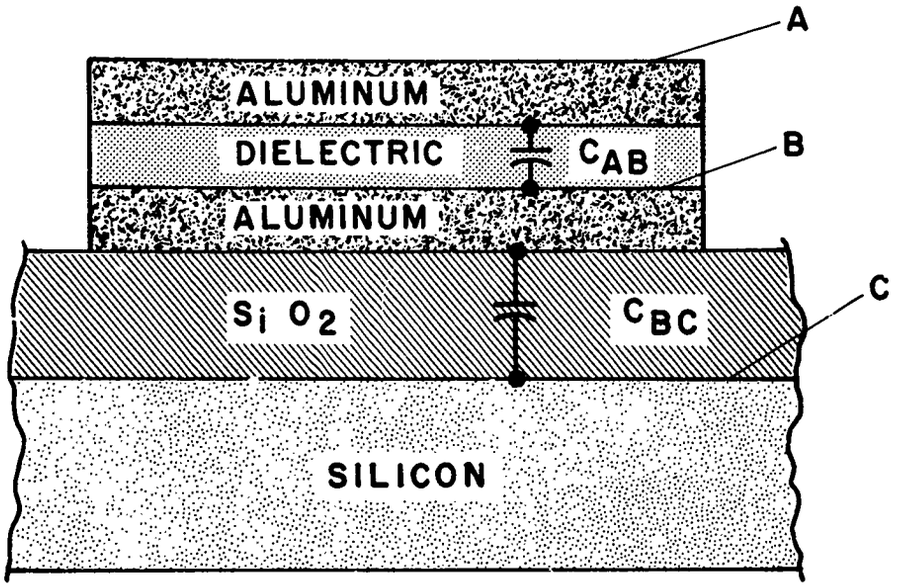
### 1.2.2 Resistors

Of the materials presently under investigation for resistors, nichrome and tin oxide have been processed with the greatest success. Nickel oxide, tantalum oxide and tantalum nitride are also being investigated.

#### 1.2.2.1 Nichrome Resistors

Nichrome resistors from 100 to 400 Ω/□ are being made on a fairly routine basis. The evaporator with the electron bombardment source is working very efficiently in depositing the nichrome films. A glass substrate monitoring strip has been added to the system so that films can now be deposited to a specific resistivity. The defining of the resistor pattern in the nichrome has been done both by etching and by reverse photoresist. So far the reverse photoresist works well only on the high ohms per square films, because this is a mechanical rupture method and the thinner films lend themselves more readily to this type of processing. Metalization of the nichrome has been successfully performed with pure aluminum deposited onto a cold substrate.

A set of fixtures for increased production of nichrome resistors is being fabricated. Continuation of etching vs. reverse photoresist method of defining the resistor pattern are under investigation. Both methods have been used in forming nichrome resistors on a 120 Mc amplifier. Some adhesion problems were encountered on the first samples, but this will be corrected by heating the substrate before evaporation.




COUPLING CAPACITOR

FIGURE 1

### 1.2.2.2 Tin Oxide Resistors

Tin oxide films, grown by the spray atomizer technique, using antimony dopant, have been used for making resistors of about 100 Ω/□. These films etched very nicely. Ohmic contacts have been made successfully by using nickel as an intermediate metal between the aluminum and the tin oxide. Experiments are presently under way to determine the best method of "passivation" for tin oxide resistors. Films of room temperature deposited silicon dioxide, reactively sputtered silicon dioxide, and aluminum silicate glass are being tested.

Tin oxide resistors are being tested separately from the 120 Mc amplifier to determine if "passivation is possible using aluminum silicate glass. Difficulties have been encountered in etching through the glass to the tin oxide. This has been evident both by microscopic examination and in electrical life tests. In the latter case at 300° storage, the "passivated" tin oxide showed large increases in resistance values as compared with unpassivated units.

### 1.2.3 Capacitors

The mask set for experimental development of capacitors has been received and is being used to develop various methods of fabricating compatible capacitors. The following outline illustrates the experimental plan. It consists of two programs, one for dielectrics formed by an electrical and chemical anodization and the other where the dielectric material is deposited by evaporation or gas vapor plating.

### 1.2.3.1 Aluminum Oxide

Some limited success has been realized in fabricating capacitors that are completely compatible with integrated circuits utilizing a new tin oxide method. Values of 1 μμf per square mil with 5 volts breakdown have been realized. No life tests have been performed on these capacitors, as yet.

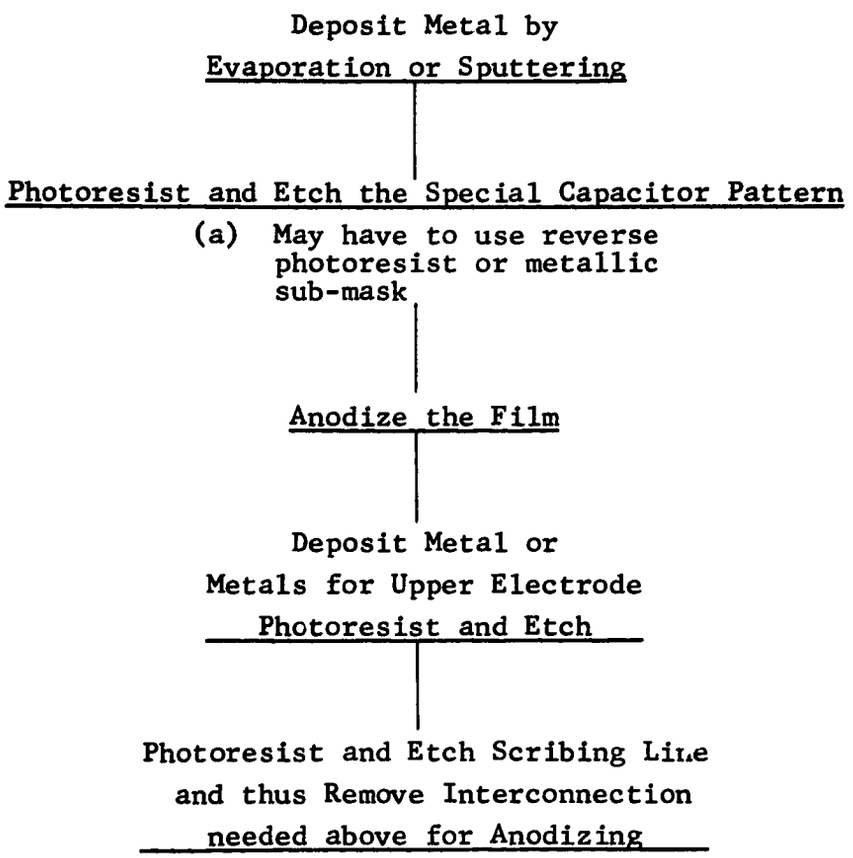
### 1.2.3.2 Aluminum Silicate and Silicon Dioxide

Studies with etching of these oxides show that we should be able to make compatible capacitors with either of these materials. There are some problems associated with photoresist step to be overcome, but this will be solved shortly.

## 1.2.4 Conclusion

Experiments are presently under way to test all the foregoing approaches to making thin film compatible capacitors. As this is a very complicated procedure, several unforeseen difficulties have arisen. These are being solved as rapidly as possible. A few capacitors have been made by the procedure under (a) "Dielectrics Etchable on Top of Aluminum," but the most useful devices will probably result from those produced by the procedure outlined under dielectrics not etchable over Al or $SiO_2$.

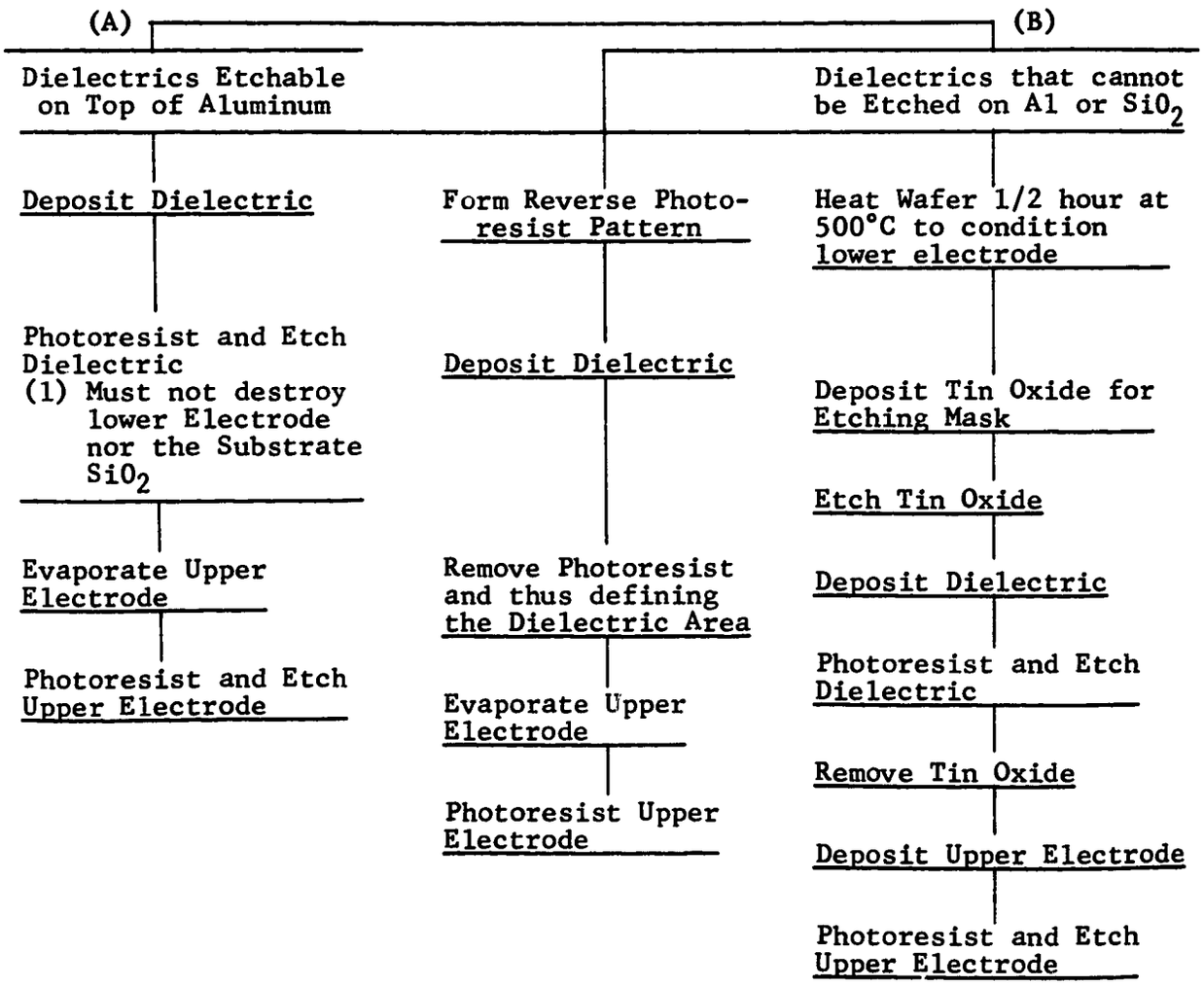
(1) ANODIZED FILMS, i.e. TANTALUM



## (2) DEPOSIT OXIDE, i.e. ALUMINUM SILICATE

Evaporate Lower Electrode Aluminum
or Aluminum and Nickel

Photoresist Lower Electrode



## 2.0 SILICON PROCESSING TECHNOLOGY

### 2.1 Process Control Investigation

A large number of wafers were completely processed during this reporting period to prove out the feasibility of the "Integral Control Pattern Concept" designed to optimize Integrated Circuit Processing methods. Several different types of circuits have been fabricated utilizing the control pattern for process control.

The circuits processed include the following:

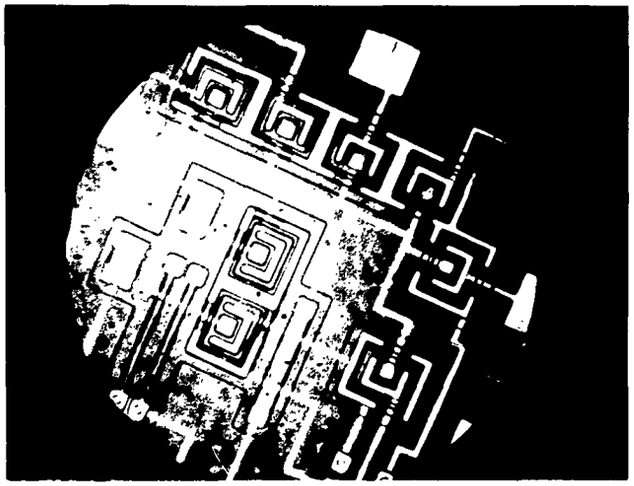
1. MECL Gate
2. MECL Flip Flop
3. MECL Half Adder

Figures 1 through 3 show photographs and circuit diagrams of the above units.

#### 2.1.1 Control Pattern

Using the Control Pattern, fast, simple and accurate techniques have been perfected for the measurement of isolation, $BV_{CBO}$, $BV_{EBO}$, $BV_{CEO}$, $BV_{CES}$ and $h_{fe}$. These measurements are carried out by operators on all wafers after all diffusions (except base diffusion) and afford a very tight method of process control.

Accurate measurement of sheet resistance prior to metallization has presented some problems due to high contact resistance in the Test Pattern areas. New techniques of sheet



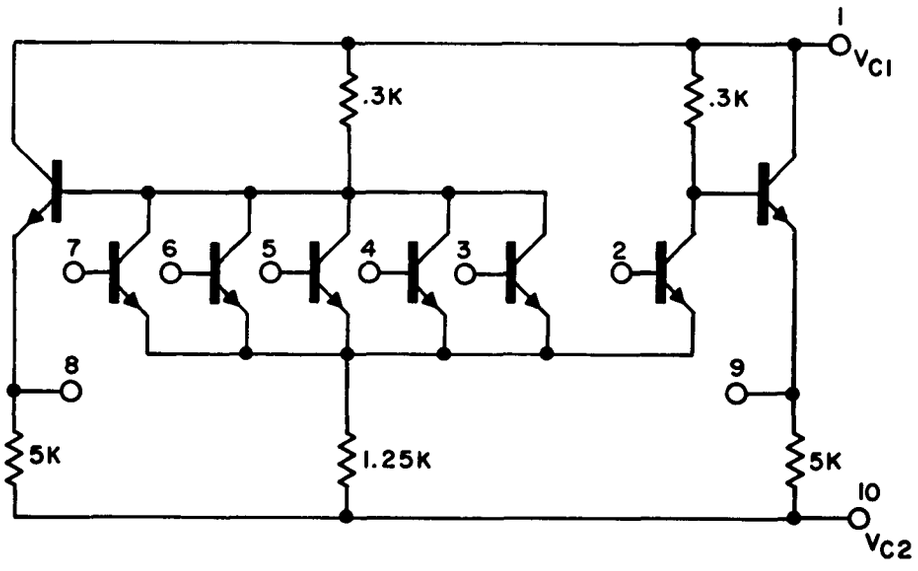
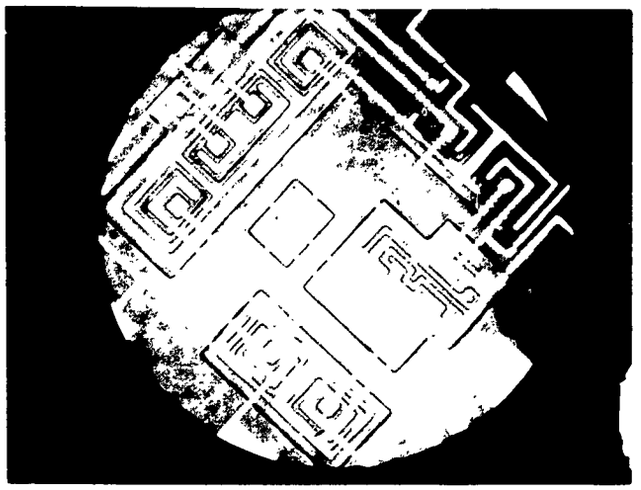



FIGURE 1
Metallized MECL Gate



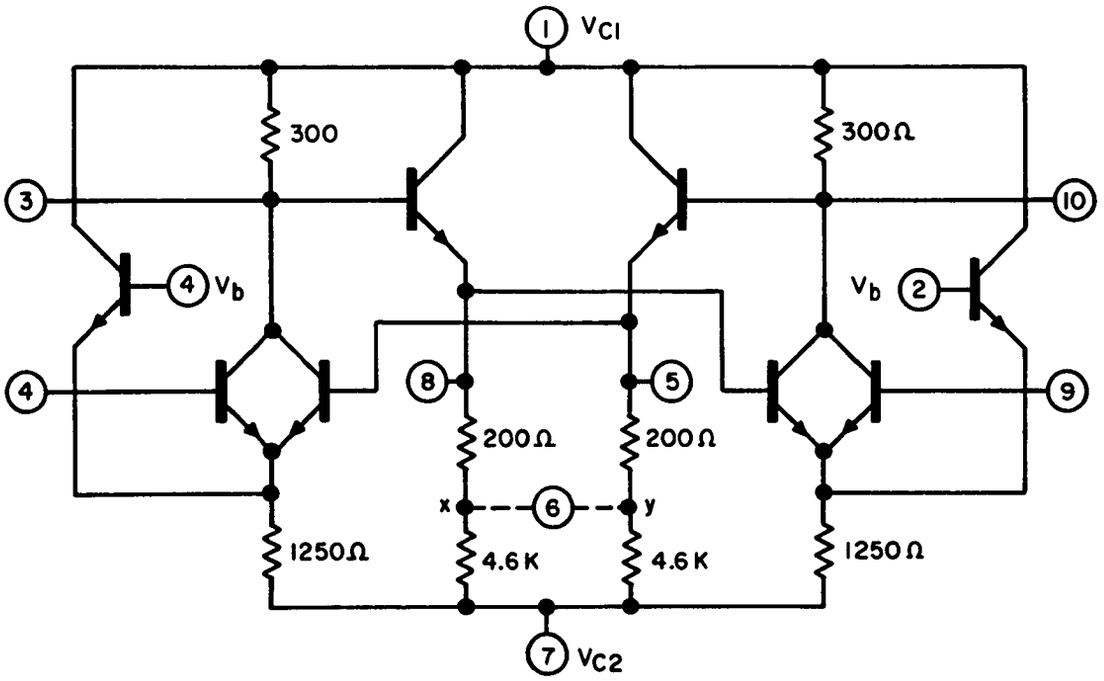
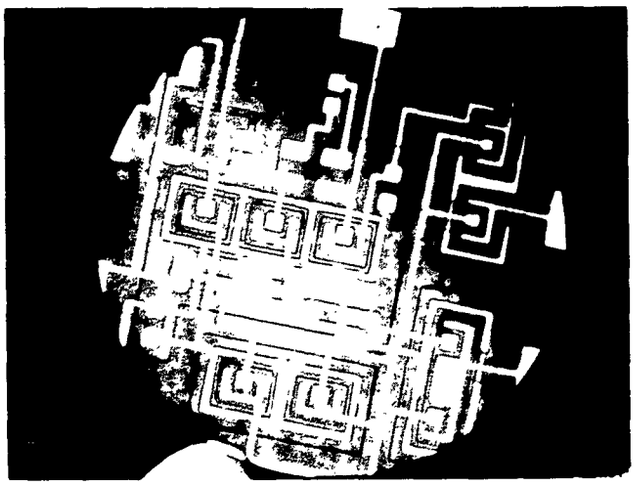



FIGURE 2
MECL Flip Flop



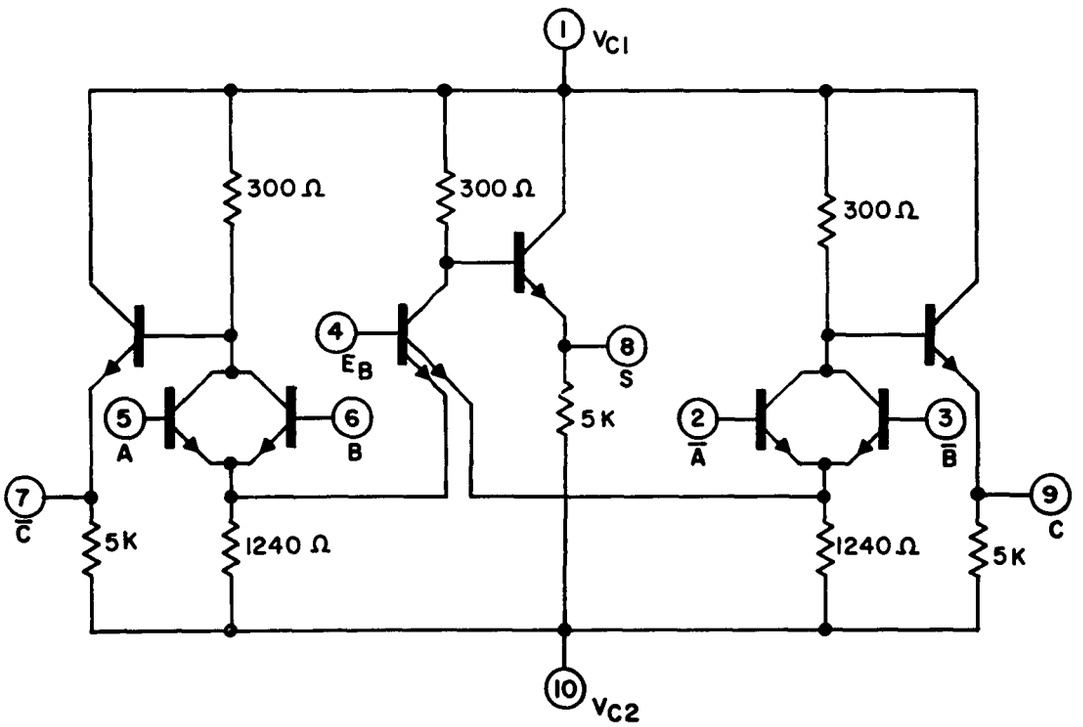



FIGURE 3
MECL Half Adder

resistance measurement are presently being developed and this measurement will be carried out on a routine basis as soon as possible.

Figure 4 shows a photograph of a completed test pattern on a wafer.

With the experience gained from the present control pattern, a new control pattern has been designed, which includes the metallic interconnections as a final process step.

The new test pattern is shown in Figure 5, with the equivalent circuit in Figure 6.

### 2.1.2 Process Optimization

The aim during this reporting period has been to define and investigate problem areas in the present Integrated Circuit Fabrication Process.

Integrated Circuits fabrication has now reached the stage where "standardization" of fabrication processes and optimization of particular process steps is desirable.

The vehicles for process studies have been detailed in Section 2.2 and shown in Figures 1 through 4.

In all cases, the smallest tolerance (from edge of emitter contact to edge of emitter base junction) is .001".

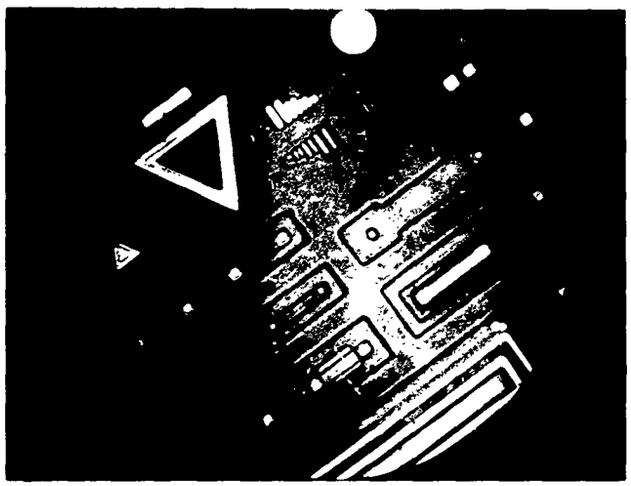
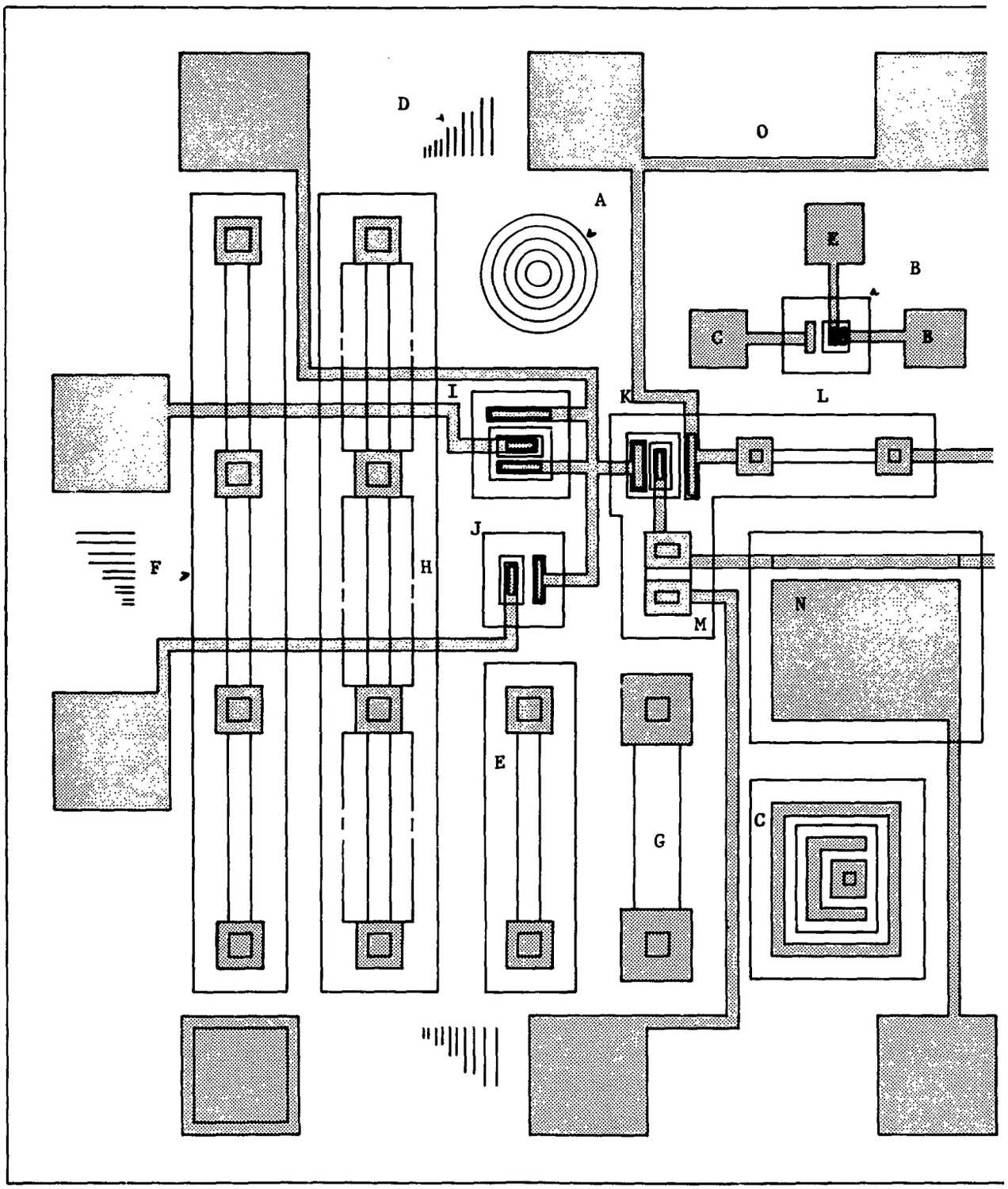


FIGURE 4
Metallized Test Pattern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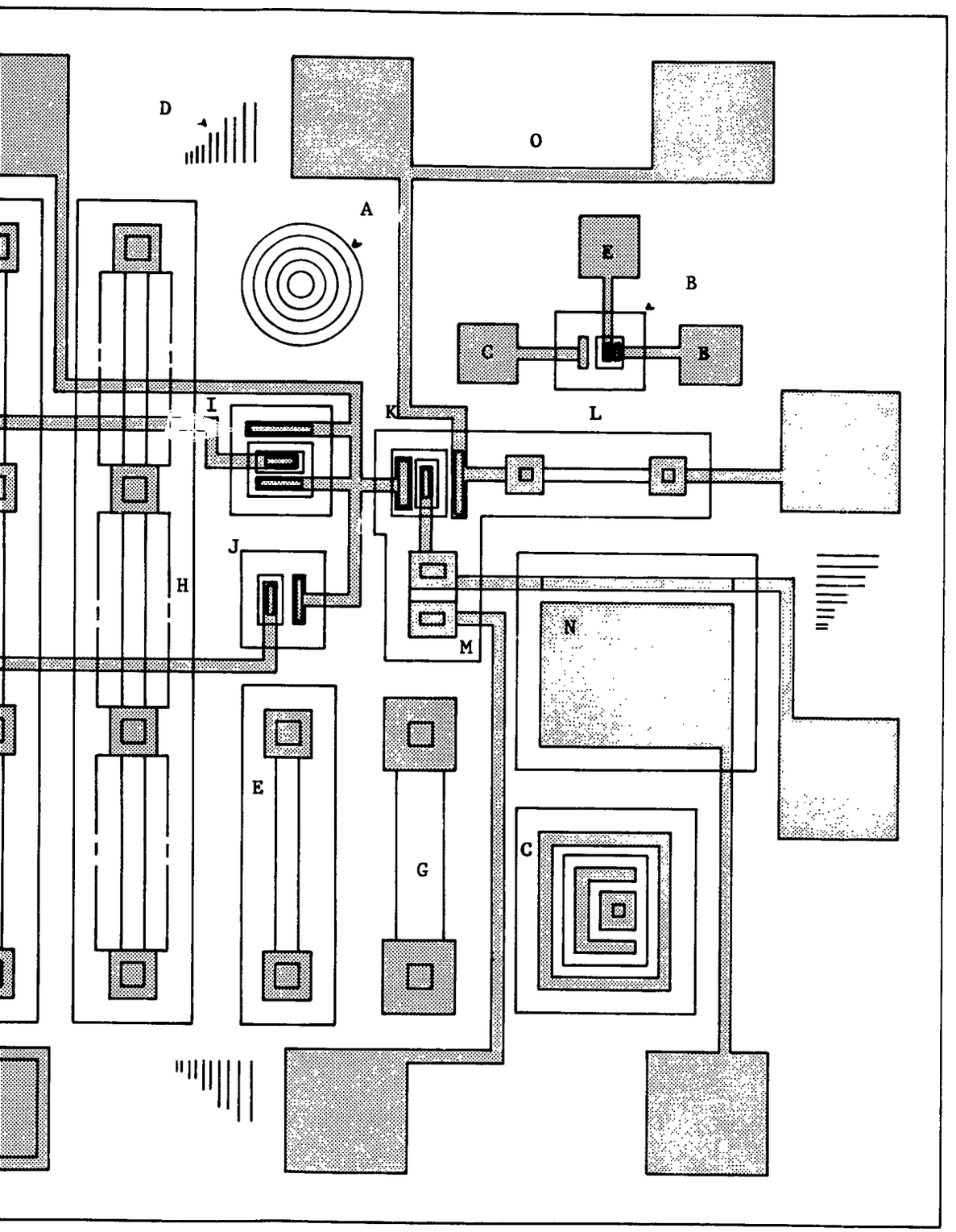
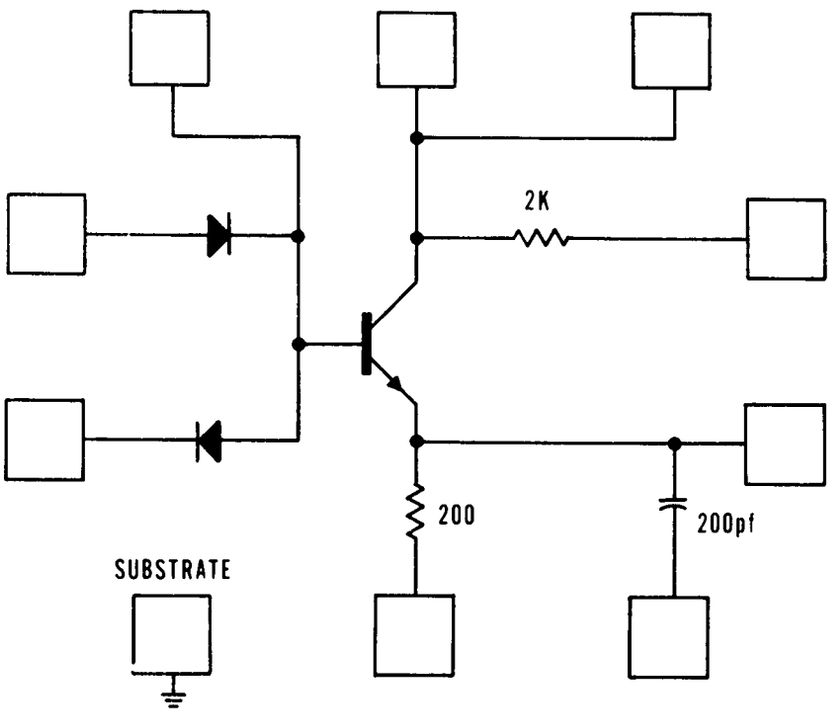



INTEGRAL CONTROL PATTERN

A. Alignment pattern
B. UHF Transistor for Process Resolution
C. Large Transistor for Process Control ($BV_{CBO}$, $BV_{EBO}$, $BV_{CS}$, $H_{FE}$)
D. Resolution Pattern
E. Base Resistivity after Emitter Diffusion
F. Base Resistivity
G. Epi Resistivity
H. Base Width Measurement
I. High Speed Emitter-Base diode for life test
J. High Speed Collector-Base Diode for Life Test
K. Standard Transistor for Life Test
L. 2 k Resistor for Life Test
M. 200 Ω Resistor for Life Test
N. Junction-type Capacitor for Life Test
O. Short Circuit Test

2

FIGURE 5




**INTEGRAL CONTROL PATTERN TEST CIRCUIT**

FIGURE 6

Critical resistors have been held to .003" and non-critical resistors to .001". Interconnecting metalization is .001".

The transistor geometry used is shown in Figure 7.

2.1.2.1 Process Description

The "standard" integrated circuit process using diode isolation is shown in Figure 8 in flow chart form.

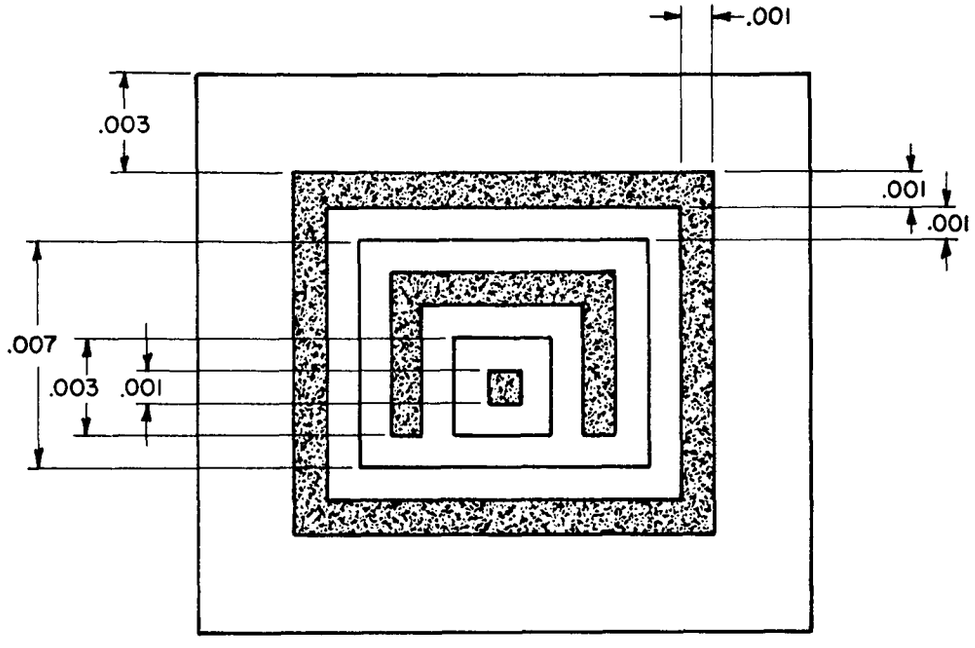
Starting material is p type silicon with a resistivity of 2-5 Ω cm. Covered with approximately 20 microns of 0.8 Ω cm of n type epitaxial silicon.

The inspection methods for incoming material depicted in Figure 8 are not at present being used. Epi thickness is presently being measured by bevelling and staining, on a sample basis. Resistivity is measured, also on samples, using a 4-point probe.

2.1.2.2 Results

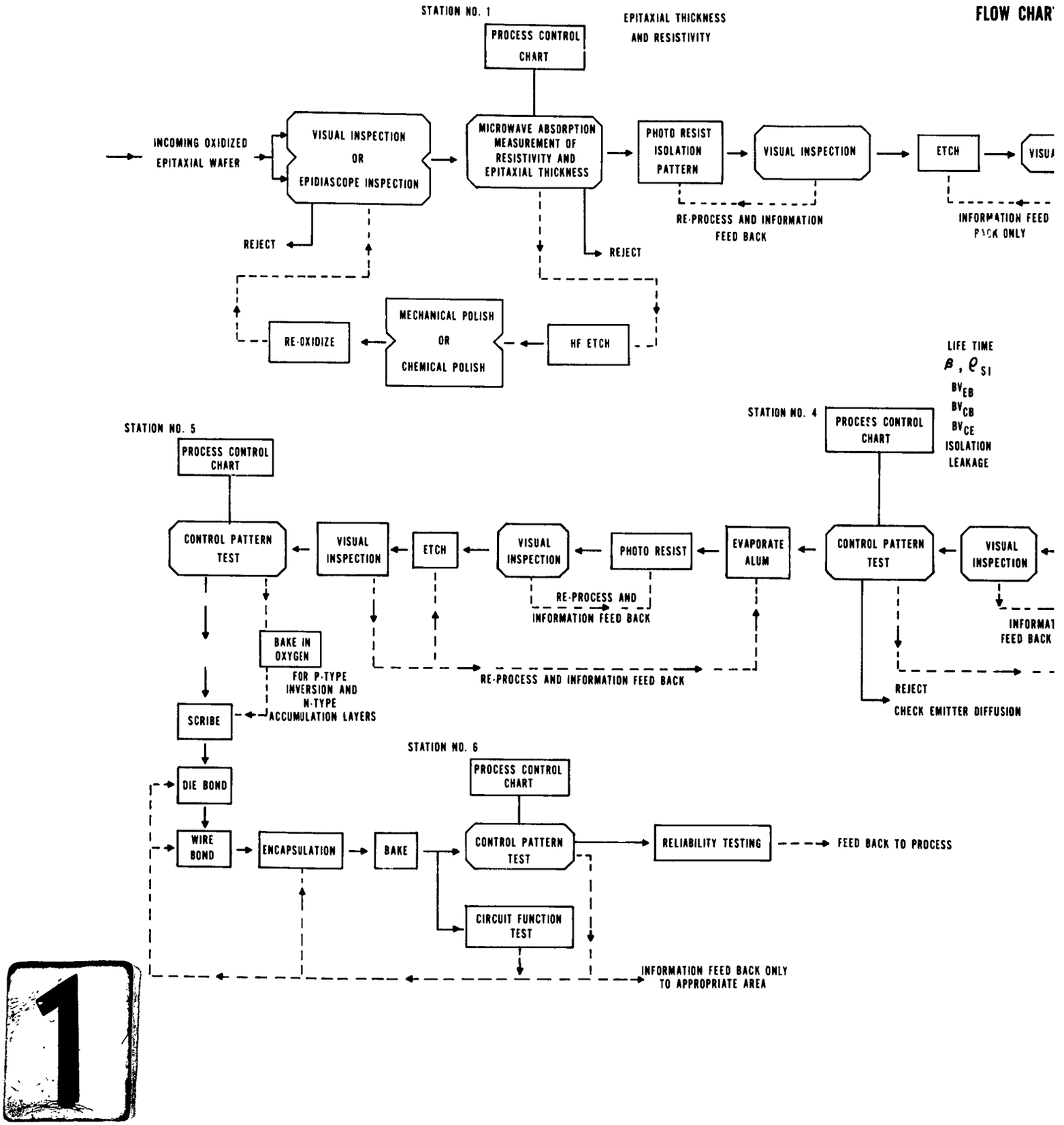
Detailed electrical results on all breakdowns, leakage and $h_{fe}$ will be given in the next report.

In general, very few accute problems have arisen with the present process. The yields have been very good. Some problems have been encountered which are being ironed out. The problem areas are described below:




All Dimensions in Inches

FIGURE 7
Plan View of "Standard" Transistor


FLOW CHART
STATION NO. 1
PROCESS CONTROL CHART
EPITAXIAL THICKNESS AND RESISTIVITY
INCOMING OXIDIZED EPITAXIAL WAFER
VISUAL INSPECTION OR EPIDIASCOPE INSPECTION
MICROWAVE ABSORPTION MEASUREMENT OF RESISTIVITY AND EPITAXIAL THICKNESS
PHOTO RESIST ISOLATION PATTERN
VISUAL INSPECTION
ETCH
VISUA
RE-PROCESS AND INFORMATION FEED BACK
INFORMATION FEED BACK ONLY
REJECT
REJECT
RE-OXIDIZE
MECHANICAL POLISH OR CHEMICAL POLISH
HF ETCH
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$BV_{CB}$
$BV_{CE}$
ISOLATION LEAKAGE
STATION NO. 4
PROCESS CONTROL CHART
CONTROL PATTERN TEST
VISUAL INSPECTION
EVAPORATE ALUM
PHOTO RESIST
VISUAL INSPECTION
ETCH
VISUAL INSPECTION
CONTROL PATTERN TEST
RE-PROCESS AND INFORMATION FEED BACK
INFORMAT FEED BACK
REJECT
CHECK EMITTER DIFFUSION
STATION NO. 5
PROCESS CONTROL CHART
CONTROL PATTERN TEST
BAKE IN OXYGEN
FOR P-TYPE INVERSION AND N-TYPE ACCUMULATION LAYERS
RE-PROCESS AND INFORMATION FEED BACK
SCRIBE
STATION NO. 6
PROCESS CONTROL CHART
DIE BOND
WIRE BOND
ENCAPSULATION
BAKE
CONTROL PATTERN TEST
RELIABILITY TESTING
FEED BACK TO PROCESS
CIRCUIT FUNCTION TEST
INFORMATION FEED BACK ONLY TO APPROPRIATE AREA

## FLOW CHART SHOWING PROCESS CONTROLS, CONTROL CHART POINTS, AND POSSIBLE CORRECTIVE ACTION

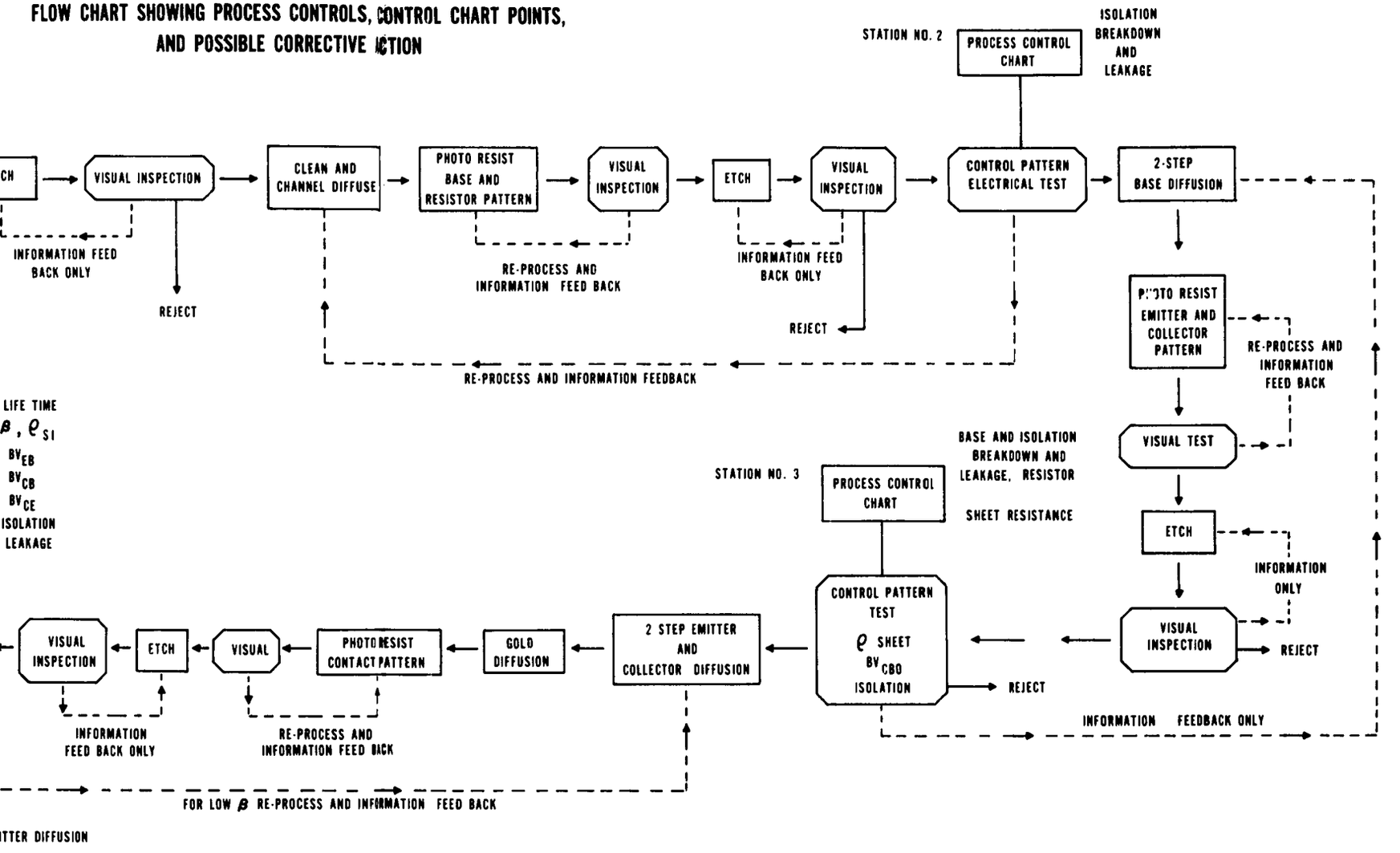



FIGURE 8

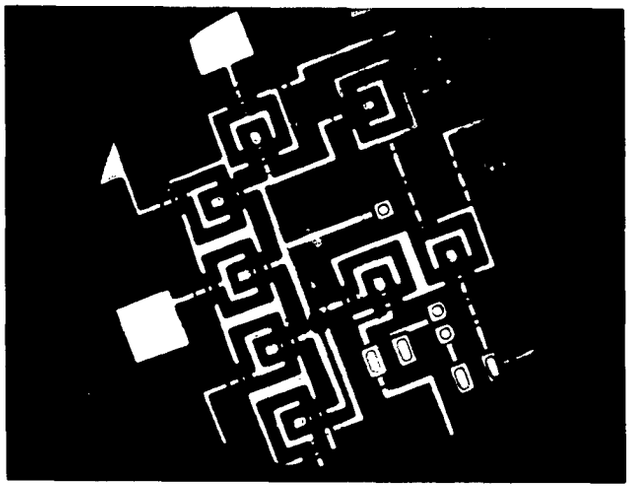
1. Staining Problems: Stains occur during two phases of integrated circuit processing, both of which are connected with selective glass removal from a previously processed wafer.

   a. In etching boro silicate glass patterns, stains develop in the etched region only on p type layers, i.e. on the etched area prior to emitter diffusion on n-p-n structures.

   b. In etching glasses containing both phosphorous and boron impurities, stains occasionally occur on both n and p type areas.

   The cause of these stains and their effect on subsequent diffusion and metalization is currently being studied.

2. Interconnection Metalizing: Some problems have been encountered with the .001" wide Al. lines. In some instances, these lines are etched through by unidentified "splashes" of etchant. (See Figure 9) Most of these splashes have been traced to pinholes in the wax mask during the "back etching" procedure. The back etching procedure has been changed, and the problem has been alleviated. However, some of the "splashes" appear to be caused by mechanisms still not fully understood. The problem is being investigated.



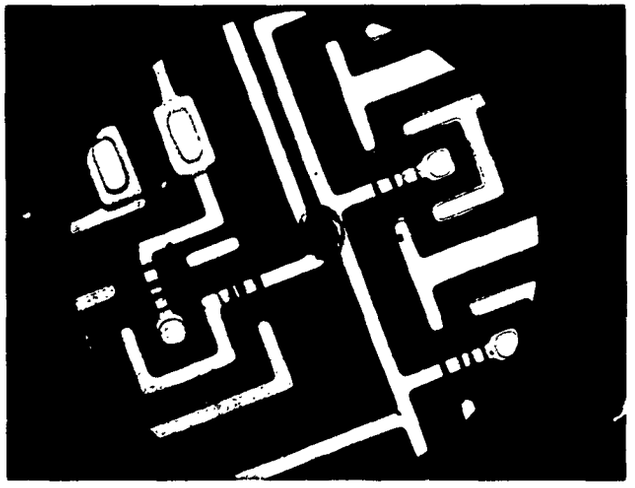


FIGURE 9
Metallization Problems

### 2.1.3 Higher Speed Circuits

The transistor shown in Figure 1 and the associated art work has been developed for non-saturating circuits with propagation delay (p.d.) times in the region of 20 nanoseconds.

During the present reporting period, an extremely small geometry mask set has been designed which is capable of propagation delay times of 5 nanoseconds. The circuit has a minimum tolerance of .0003" which is approaching the limit of known techniques using conventional photolithographic techniques.

## 2.2 Diffusion-Epitaxial Techniques to Obtain Low Collector Series Resistance

### 2.2.1 Introduction

One of the prominent obstacles to the design of integrated circuits in the monolithic chip form, has been the high collector series resistance. This resistance is inherent in the "present state-of-the-art" technology for both diode and resistivity isolation schemes. The collector series resistance can be changed in three ways, namely:

1. Increasing the thickness of the collector region.
2. Decreasing the resistivity of the collector region by doping the collector heavier.
3. Decreasing the resistivity of the collector region by utilizing an epitaxially grown collector with a "buried" diffusion region.

The first two methods, although feasible, are undesirable in that they increase the channel diffusion, thereby, limiting the geometrical tolerances available. Furthermore, lowering the resistivity of the collector region is limited by the capacitances required. To overcome these difficulties, the "buried layer" technique is under investigation.

### 2.2.2 The Buried Layer Technique

Essentially, the "buried layer" technique consists of diffusing a region into the substrate prior to the deposition of the epitaxial layer. Then, during epitaxial growth and the subsequent base and emitter diffusions, the pre-epi diffusion will out-diffuse into the epitaxial collector to give a low collector series resistance path that will drop $R_{SAT}$. The problem that exists is mainly one of control to produce a given $R_{SAT}$ that is compatible with the other desired device characteristics. At present, three experiments are being conducted on a comparative basis as to which can give an effective control of $R_{SAT}$.

The simplest technique, of course, is to introduce into the substrate an impurity source which will out-diffuse toward the surface, but will not diffuse into the base region. This is shown in Figure 10. Note the impurity source must be localized to permit relatively easy compensation in the isolation region. Normally, this structure is built for an NPN transistor with a P-type substrate. This means that boron is used as the compensating impurity of the epitaxial layer to form the isolation channels. The out-diffusion from the buried layer must occur at a slower rate than the channel diffusion used to form the isolation. Experiments are being conducted on how this can be accomplished by

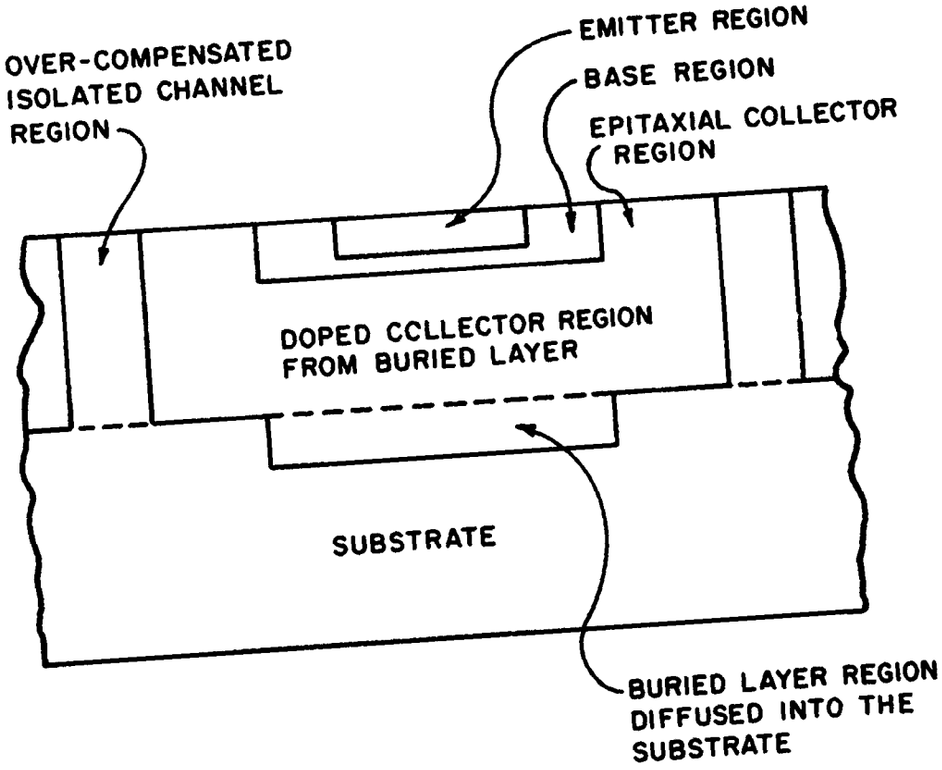



FIGURE 10
CROSS-SECTION OF A DIE WITH A SINGLE BURIED LAYER

varying the concentration source of a phosphorous buried layer at the epi-substrate interface, and by using arsenic to take advantage of its lower diffusion coefficient.

## 3.0 UHF TRANSRECEIVER DESIGN AND FABRICATION

Model I of the 120 Mc transreceiver was delivered in October as reported in the Sixth Quarterly Report. Investigations were carried on during this period to develop a series of functional electronic blocks capable of performing in Model II of the transreceiver which will utilize single chip design employing thin film components deposited on a silicon substrate.

## 3.1 Summary

Evaluations on the breadboard model of the 120 Mc receiver using the new Beta C amplifier configuration and single conversion have been completed and substitutions of a few hybrid integrated circuits of this configuration have been made. A FEB circuit on a 100 mil square silicon die has been designed for this circuit and a mask set started. This FEB is suitable for the 12 Mc IF section.

A second FEB for 120 Mc and higher frequencies is being evaluated and designed and has been drawn up for mask set fabrication.

The basic part of the Beta C circuit in FEB form can be derived from a FEB MECL logic unit. Some very interesting tests have been made on this circuit. Indications are that there is considerable assurance the new FEB circuits will perform satisfactorily as the result of these tests.

Construction has started on two ruggedized versions of the 120 Mc transreceiver for delivery to the Air Force within six months. Motorola-Chicago has agreed to design ruggedized cases, antenna and reliable switches for these models.

## 3.2 Interim Work on 120 Mc Transreceivers

Using breadboard approaches, several new developments have been evaluated in relation to not only the 120 Mc transreceiver

vehicle, but also to ultimate fabrication in FEB forms.

A considerably altered and simplified circuit approach to the receiver section of this vehicle has been made, utilizing single conversion to 12 Mc I.F.

Further developments in compatible crystal filter systems indicate that a 12 Mc crystal filter mounted in no more than three consecutive TO-5 packages is feasible. In this case, the first package will contain the input transformer and balancing networks, the second,package, the four section crystal assembly, and the third output coupling assembly.

Such a crystal filter will be used with either RC coupled broadband amplifiers or LC coupled narrow band amplifiers. In both cases, the new emitter coupled RF amplifier configuration, discussed elsewhere in this report, will be utilized.

This configuration, shown in Figure 1 will be assembled in the TO-5 package in the FEB form, shown in Figure 2.

The over-all ruggedized transreceiver vehicle design will include:

1. All FEB ruggedized designs of the circuits.
2. All circuits in TO-5 packages.
3. All LC coupling elements either in TO-5 packages or in a space factor of similar configuration.

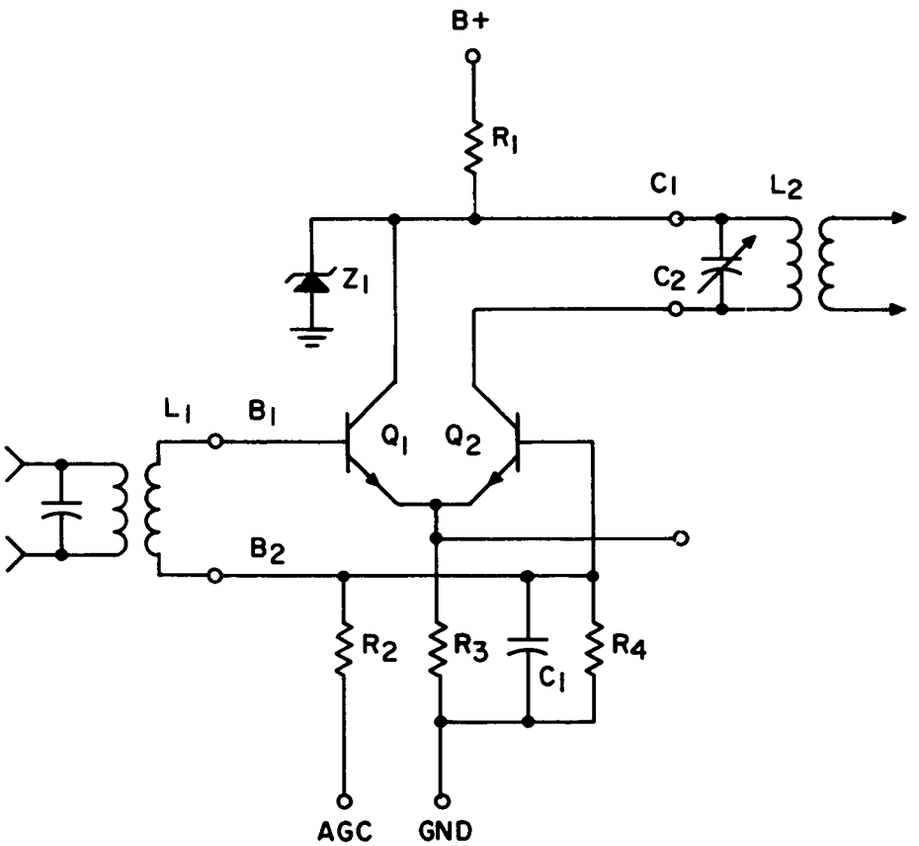



FIGURE 1. SCHEMATIC OF PROPOSED FEB

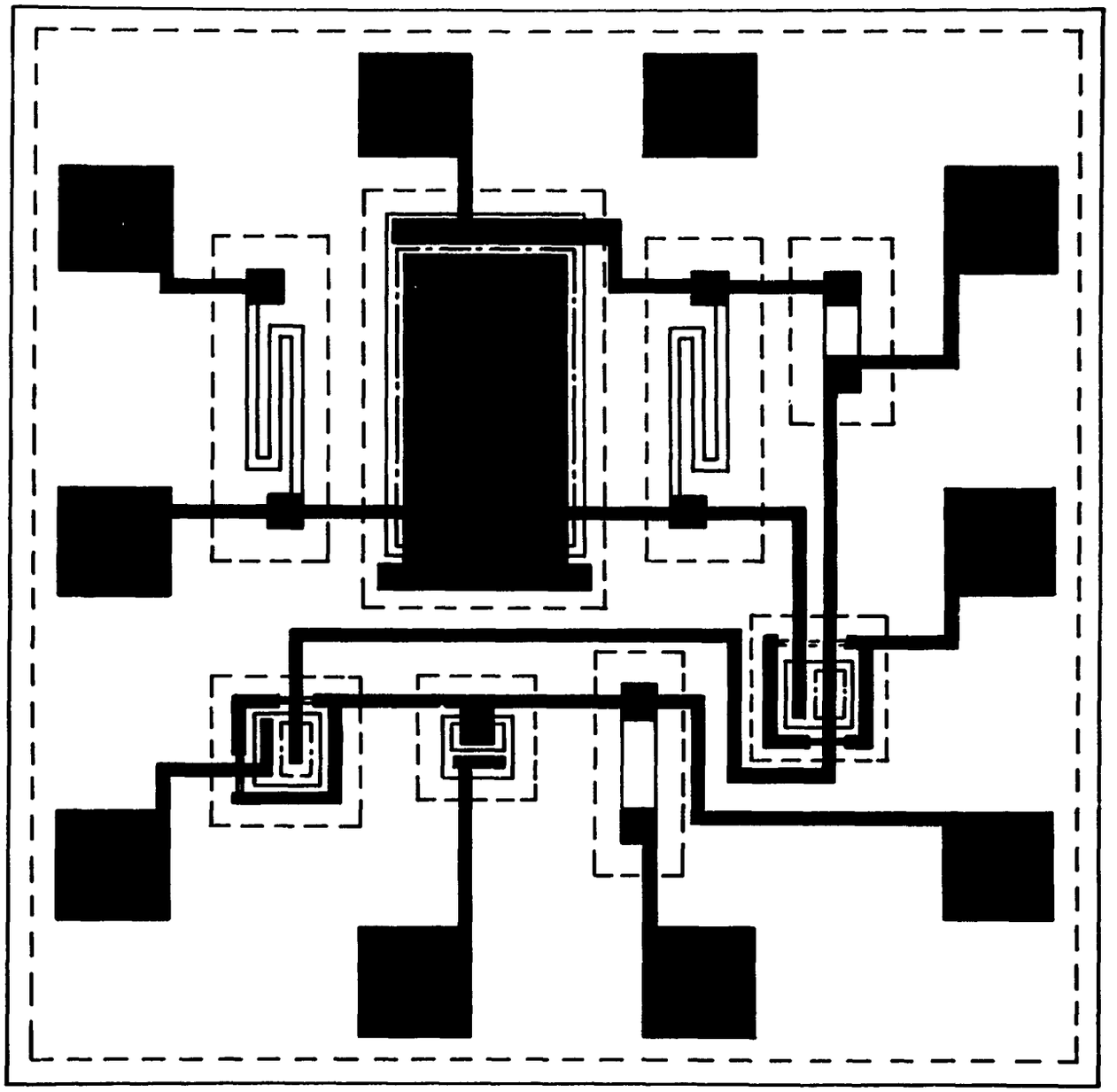


FIGURE 2

FEB LINEAR AMPLIFIER DESIGN EQUIVALENT TO FIGURE I

4. A ruggedized special package with proven mechanical and switching features of the URC transreceivers. This design will provide for complete integration into the TO-5 cans of all circuit elements except two crystals, and the essential trimmer capacitors.

The work presently underway on this phase is:

1. Assembly of Hybrid Linear Amplifier stages in TO-5 cans.
2. Design of basic circuit board for assembly.
3. Design of transmitter system utilizing similar circuits.
4. Design of suitable container package along military standards.
5. Design and fabrication of 12 Mc Crystal Filter Elements.

## 3.3 Evaluation of Functional Electronic Block Linear Amplifier

### 3.3.1 Considerations

In the design and evaluation of FEB linear amplifiers, there is very little precedent and practically no analytical data to establish just how these will perform in practical circuits. Semiconductor theory may predict that they will behave in a certain way, and approximately they probably will. However, when the circuit engineer finally gets one in an operating circuit, he

can have much more confidence that the theoretical predictions are fact.

The one phenomenon which has been predicted in a circuit completely formed in a single block is parasitics. These take the form of capacitances, resistances and sometimes semiconductor interaction. These same interactions are also of significance in conventional circuitry, although most times probably to a much lesser degree.

Quite recently it became apparent that it would be possible to evaluate by actual measurements an essentially complete FEB linear amplifier, even before such time as a complete amplifier of this nature has been built. The following sections of this report are devoted to the findings, as of this writing, of this effort.

### 3.3.2 High Frequency Linear Amplifier for FEB Design

A new high frequency amplifier circuit recently proposed by the Motorola Integrated Circuits Application group, has been selected as the best approach for full integration into Functional Electronic Block (FEB) at this time. This is in line with the Air Force interest in FEB linear circuits and flat package designs.

Accordingly, this circuit, the emitter coupled RF amplifier, also sometimes known as the Beta C circuit, shown conventionally in Figure 1 has been laid out and a mast set started. This layout is shown in Figure 2. The dotted line in Figure 1 indicates the circuitry included in the FEB design.

The circuit function is as follows:

$R_1Z_1$ provides a collector decoupling network and holds the collector supply level at 8 volts due to the zener control action of $Z_1$, which in the FEB design is an emitter base transistor junction.

Transistor $Q_1$ and $Q_2$ are small junction area high frequency types. $Q_1$, whose base is driven by the input signal provides an emitter follower action and drives the emitter of $Q_2$ through the common unbypassed emitter resistor $R_2$. The base of $Q_2$ ($B_2$) is biased to ground through $R_3$ and AC bypassed by capacitor $C_1$. The conducting bias, in the form of an AGC voltage is applied through $R_4$ to both bases simultaneously through the DC path provided by the secondary of the coupling transformer $T_1$. Hence, capacitor $C_1$ also serves the second function of AGC decoupling. The bypass function of $C_1$ can be shown to be, frequency wise, a function of $C_1$X Beta, where Beta is the current gain of transistor $Q_2$. This means essentially that for any given frequency, $C_1$ can be twenty or more times smaller than the bypass elements in other kinds of amplifiers, such as the conventional grounded emitter types. Since in FEB circuits the silicon block surface is limited and unless the block is made uneconomically large, there is just no room for either very large, or very many capacitors. The capacitance per unit area is approximately 1 pfd per square mil of surface. With the space required for the rest of the circuit, this allows comfortable space for only one 500 pfd capacitor on the 100 mil square silicon block (Figure 2).

The collector load is a tuned resonant transformer $T_2$. The resonant frequency is determined by the transformer L and

parallel capacitor $C_2$. Part or all of $C_2$ may be the inherent collector to substrate capacitance, due to the collector isolation diode in the FEB. Hence, with this arrangement, this parasitic capacitance Cp, is "tuned out" as a high frequency load, becoming instead contributory to the high frequency gain.

The tuned intercoupling transformers, $T_1$ and $T_2$ not only establish a bandpass characteristic, but also provide for efficient impedance matching into following loads.

### 3.3.3 Nature of Tests Made on the Emitter Coupled Amplifier

A B+ voltage of 8 volts was used to simulate the zener control (this was not used in these tests) and the AGC voltage furnished from another variable supply.

Signals were injected from a variable frequency generator and the output gain, frequency spread and peak frequency were monitored on an oscilloscope using various choke values for $CH_2$, Figure 3.

Since no other capacitance was applied across the choke, the LC resonance obtained is virtually all due to the parasitic shunt capacitance Cp, within the block. This enables a computation of the inherent Cp within this particular FEB.

The data obtained at the peak gain frequencies is given in Table 1. The gross resonant C is calculated from the known f and L values.

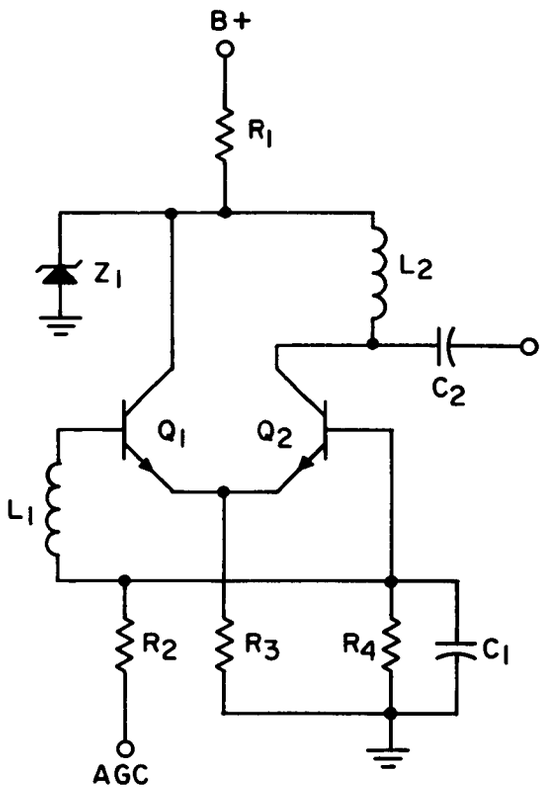



FIGURE 3. CHOKE LOADED MECL AMPLIFIER TEST CIRCUIT.

TABLE 1

Measurements on FEB Linear Amplifiers (MECL)

Test Conditions: $V_{CC}$ 8 V
$I_C$ 3 Ma
AGC Voltage - To 3 Ma

A. Gate Modified Amplifier with 3.3 uhy choke, $CH_2$.

| Unit No. | Resonant Frequency Mc | Max. Gain at Resonance D.B. | AGC for 3 Ma Volts | Cp CALC. pfd |
|---|---|---|---|---|
| 1 | 17.5 | 31.0 | 20 | 24 |
| 2 | 15.5 | 33.0 | 6.5 | 32 |
| 3 | 15.0 | 29.0 | 11.0 | 34 |
| 4 | 13.0 | 20.0 | 6.5 | 46 |
| 5 | 15.5 | 35.0 | 7.2 | 32 |
| 6 | 16.0 | 33.0 | 6.5 | 30 |
| 7 | 16.5 | 35.0 | 6.5 | 28 |

B. Same Units & Conditions with 1.0 uhy, $CH_2$.

| | | | | |
|---|---|---|---|---|
| 1 | 30.7 | 30.0 | 21.0 | 24 |
| 2 | 27.7 | 28.5 | 7.0 | 33 |
| 3 | 25.1 | 22.5 | 11.5 | 41 |
| 4 | 27.2 | 18.0 | 6.5 | 35 |
| 5 | 27.2 | 28.5 | 7.2 | 35 |
| 6 | 27.2 | 28.5 | 6.6 | 35 |
| 7 | 28.3 | 30.0 | 6.6 | 32 |

In the FEB amplifier design, Figure 2, smaller transistors (13 x 13 = 169 $mils^2$) will be used. This should reduce the effective Cp by one-half.

The data in Table 1 appears to indicate certain factors:

1. Four units, No.'s 2, 5, 6 and 7 are quite consistent in both tests and in all categories.
2. Units 1, 3, and 4 are at variance; 1 and 3 with abnormally high AGC voltage requirements and 4 with low gain.
3. Since there have been only these seven units available for test at this time, it is difficult to say which are the normal units. However, the relative consistency of the four above mentioned units appear to be the expected behavior and they are tentatively classed as the "normal".

### 3.3.4 Temperature Effects on the FEB Parasitic

The Cp in the FEB circuit is unavoidably part of the LC tuning capacitance in this system. Also, unavoidably it will change, as all semiconductor parameters do, with temperature and other operating conditions.

Further, it can change in at least two ways:

1. In its absolute capacitance value
2. In its effective circuit Q

Semiconductor theory predicts that there should not be any significant change in capacitance of a junction with temperature, nor of the circuit Q. However, since the FEB amplifiers are new and somewhat unknown quantities, a series of temperature performance checks was decided on.

In order to evaluate these conditions, the set-up of Figure 3 was placed in a temperature chamber and the performance data measured at four temperature points: -30°C, 0°C, room temperature (25°C) and 75°C. These runs were made with two choke values at $L_2$: 3.3 uh and 1.0 uh.

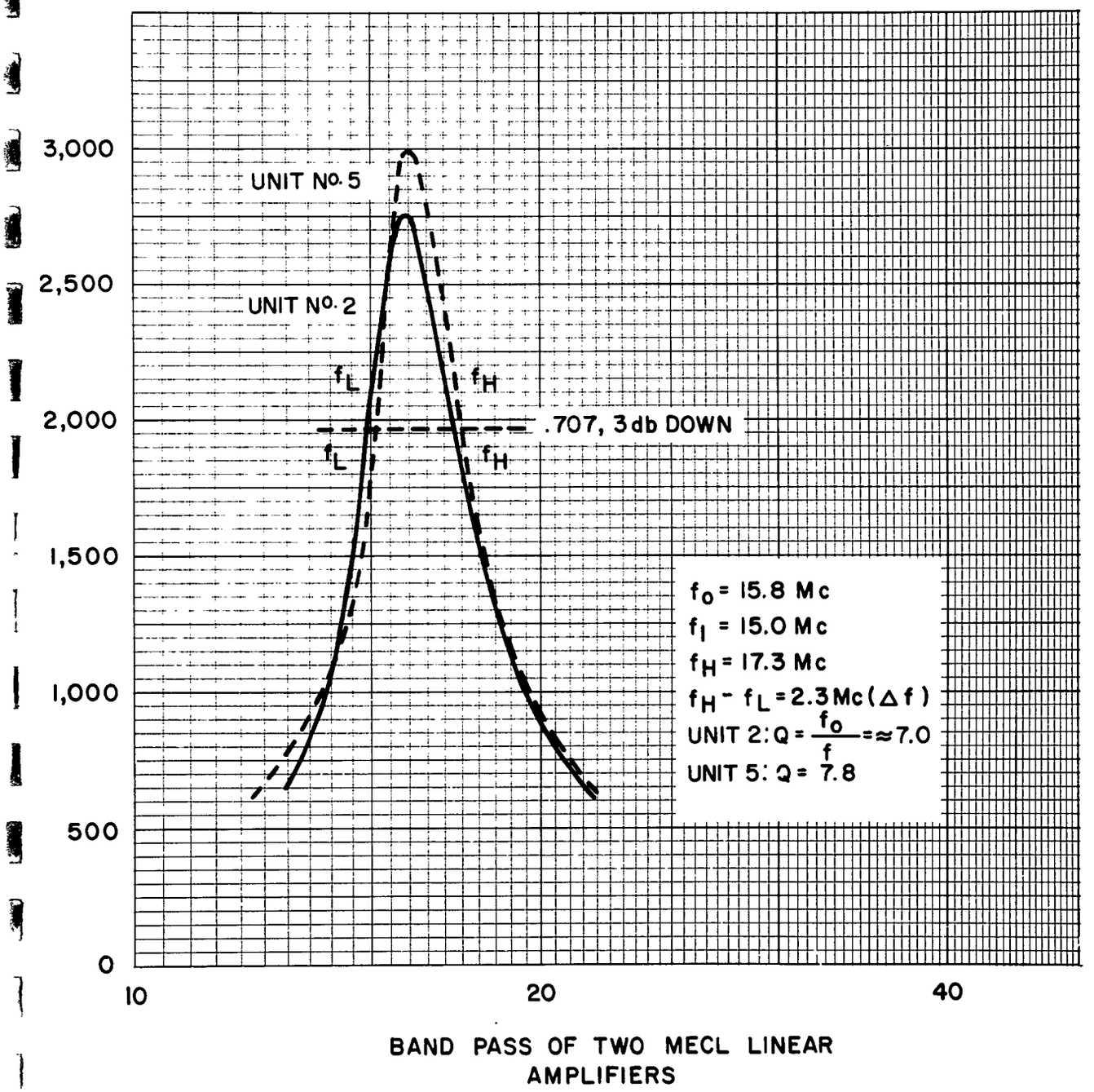
The data obtained is plotted in the curves of Figure 4. These curves are plotted as DB gain versus frequency.

Two general situations are shown in these curves.

1. There is a slight shift of peak resonant frequency toward the high frequency side with lowering temperature.
2. There is an apparent increase of the circuit Q which appears to result in greater resonant gain at the lower temperatures.

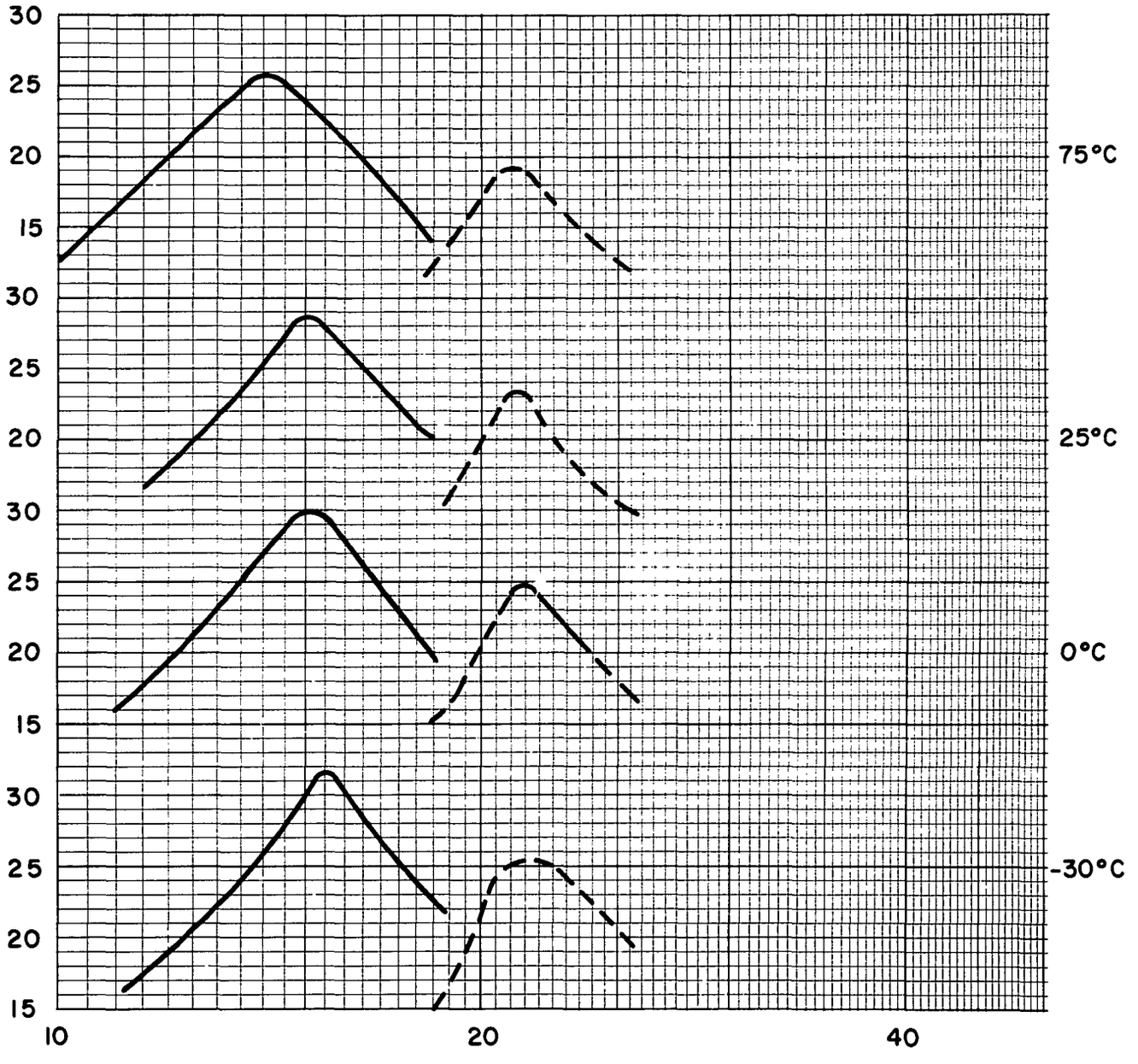
It can be shown that the small frequency shift is almost entirely due to the $T_c$ of the inductor core material used, indicating that the resultant FEB capacitance does not appreciably change with temperature.

The change in Q or whatever phenomenon is causing a higher resonant gain at low temperatures where the transistor




BAND PASS OF TWO MECL LINEAR AMPLIFIERS

FIGURE 4




LCp RESONANCE WITH TEMPERATURE

FIGURE 4

actually has less gain, is not as easily explained. Available data on the core Q with temperature, nor the resistance change in the inductor wire appear sufficient to account for the phenomenon. One explanation appears to be that due to the lower activity of intrinsic and extrinsic carriers within the semiconductor at low temperatures, the general Q of the circuit as a whole is improved.

Unquestionably a more thorough explanation of this and other circuit phenomena encountered in FEB circuits will be forthcoming as the study progresses.

## 3.4 The Performance of a Monolithic 12 Mc I.F. Strip

### 3.4.1 Introduction

This demonstration vehicle contains eight of the monolithic silicon FEB emitter coupled amplifier stages. These stages, in association with a small complement of hybrid integrated circuits or conventional components, provide all of the various stage functions in the strip.

These are: Three LC coupled 12 Mc RF amplifiers; one mixer-amplifier stage; one 11.545 crystal controlled local oscillator; two 455 Kc RC coupled amplifiers, and one biased double diode detector.

These stages are completely and individually mounted in TO-5 packages in the final models at present under construction. In these mounts, diffused resistors, oxide and junction capacitors, and miniature ferrite toroidal chokes are incorporated. In the

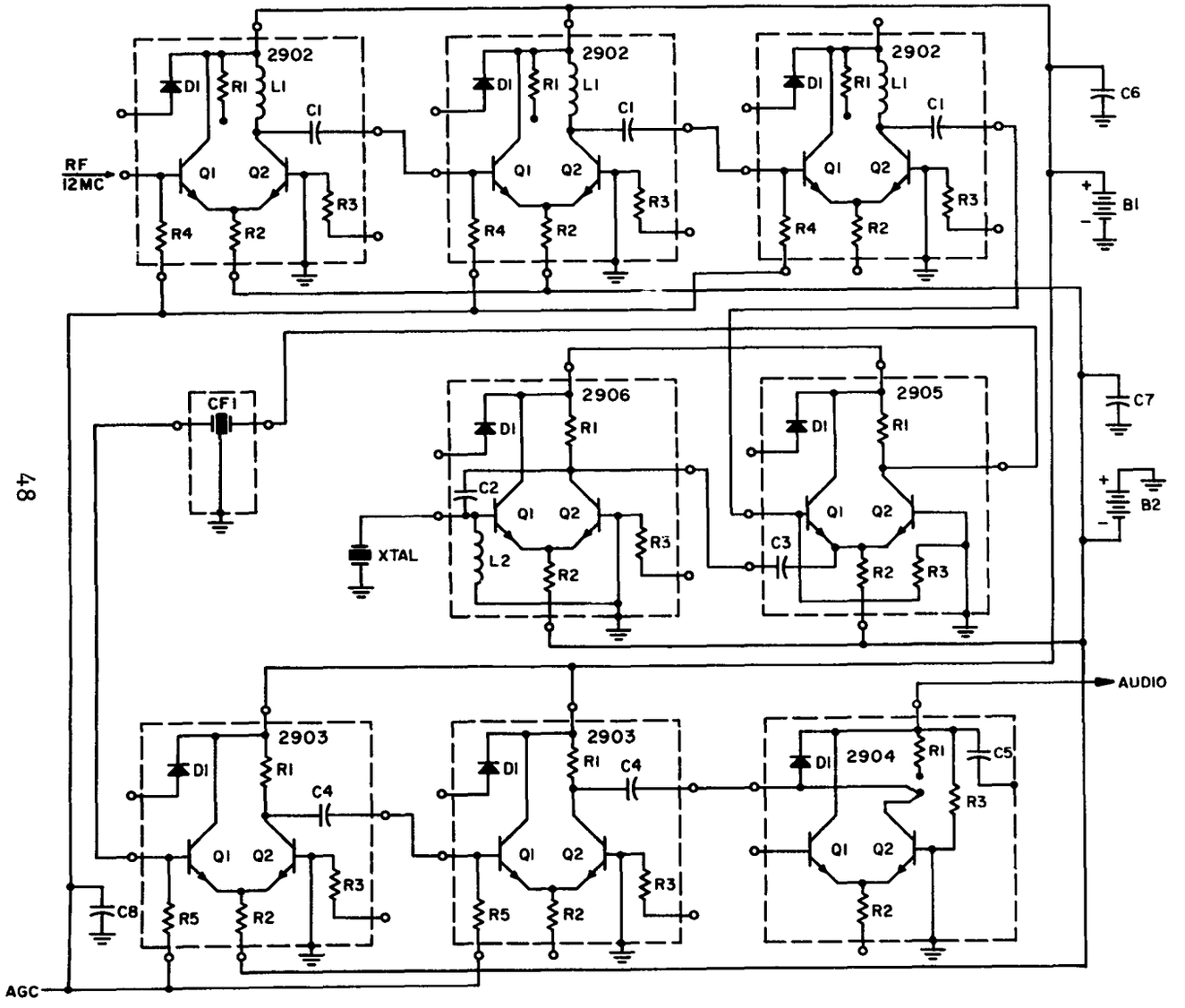
model on which these measurements were made, the extra components of miniature conventional type were for the most part mounted under the low form TO-5 cans housing the FEB blocks, using conventional miniature capacitors, resistors, along with the toroids where required.

A ninth TO-5 package in the strip houses a 455 Kc ceramic resonant filter. This filter, inserted between the mixer stage and the first 455 Kc amplifier, provides some selectivity as well as improving the signal-to-noise ratio. However, the main selectivity determining element in a receiver incorporating this strip would be a 12 Mc crystal filter, inserted between the head-end amplifier, mixer, oscillator system and the gain strip output.

The entire circuitry complement, as shown in the schematic of Figure 5, is mounted on a special two sided circuit board 1.25 inches square. Besides the nine TO-5 mounts, there are four conventional components which appear. Three of these are miniature tantalum capacitors which bypass the three supply lines (B+, B- and gain control) to ground, and a miniature glass encapsulated crystal element for the control of the 11.545 Mc local oscillator.

### 3.4.2 A Demonstration Package for the 12 Mc Gain Strip

In order to facilitate the demonstration of this strip, it has been mounted in a special chassis with a built-in power supply composed of two 4.2 volt mercury batteries, and a battery switch.




DOTTED LINES INDICATE TO-5 PKG'S

ELEMENTS IN ALL F.E.B. STRUCTURES
- DI - DIODE
- RI - 1.6K
- R2 - 750Ω
- R3 - 18K
- Q1 & Q2 - 2N834 EQUIV

ELEMENTS NOT IN F.E.B BUT IN TO-5
- R4 - 2.8K
- R5 - 4.7K
- L1 - 5μH
- L2 - 3.9μH
- C1 - 330pf
- C2 - 10pf
- C3 - 65pf
- C4 - 680pf
- C5 - 3000pf
- CF1 - 455KC CERAMIC RESONANT FILTER

ELEMENTS NOT IN TO-5
- XTAL - 11.545Mc MINIATURE CRYSTAL
- C6, C7, C8 - LOCAL BYPASS CAP. 0.5-1.0μf
- B1, B2 - 5V

TO-5 PACKAGE DESIGNATIONS
- 2902 12 Mc AMPLIFIER
- 2903 455 Kc " "
- 2904 DETECTOR
- 2905 MIXER
- 2906 LOCAL OSC. 11.545 Mc
- CF1 455 Kc CER. FILT.

12MC IF STRIP

Figure 5

A screwdriver operated potentiometer mounted inside the chassis, provides for balancing the battery voltages. A knob operated gain control for sensitivity adjustment is provided atop the chassis. This adjusts the gain of the strip satisfactorily for approximately 50 db range of signal strength.

A BNC connector is provided for cable connection to a suitable signal generator, such as the HP 606A and a second output BNC connector for an oscilloscope or distortion meter readout. Also provided atop the chassis are two feed-throughs to ground and detector output for convenient attachement of oscilloscope probles, etc.

The circuit board is mounted under a transparent panel in the chassis top, and may be visually observed on the underside also, through the open bottom of the chassis.

The following tests and evaluations have been made on this assembly:

Sensitivity: Using a signal generator with 1 Kc, 50% modulation and a HP 330C distortion analyzer on the input and output respectively, the sensitivity test of signal + noise + distortion at 6 db down, was made at 2 μV input to the strip.

Selectivity: No measurements of selectivity have been made, since the crystal filter element has not been included in the model.

In the case of the strip without this filter, any selectivity evaluations would be meaningless, since the only

selective element incorporated is the single ceramic resonant filter, whose purpose is more to improve the gain-bandwidth in this section of the strip, than to establish over-all selectivity.

Power Gain: An approximate but fairly close estimate of over-all power gain has been made and appears to be about 85 to 90 db. This test was made using the measured input impedance of 1000 ohms at 12 Mc as estimated by substitution techniques, and the effective 6000 ohm output impedance of the detector. A 90% 1 Kc modulated 12 Mc carrier was injected at about 10 μV level, and the output R.M.S. voltage measured. The input and output power can thus be calculated from $\frac{E^2}{R}$.

### 3.4.3 Gain Control

An AGC has not been applied to this demonstration. The gain control action is executed by a knob controlled rheostat. This sensitivity level must be adjusted for best undistorted signal output for various input signal levels.

Table II below gives the approximate position of the control-knob pointer in terms of several arbitrary signal input levels. In making this table, the terminated (56 Ω) HP 606A generator was adjusted for 50% modulation, 1 Kc signal, and best resonance at 12 Mc. The 1 Kc detected output signal was observed on an oscilloscope.

TABLE II

| Input Level μV | Sensitivity Control Setting |
|---|---|
| 1 | 7.6 |
| 2 | 7.4 |
| 6 | 6.0 |
| 20 | 4.5 |
| 70 | 3.7 |
| 200 | 3.3 |
| 700 | 2.0 |
| 2000 | 1.2 |
| 7000 | 0.2 |

### 3.4.4 Over-All Strip Noise Figure

Since this may well be the first system using as great a precentage of FEB monolithic block circuits in a receiver structure, some noise estimates in comparison with conventional approaches should be interesting. At this writing, these noise evaluations have not been completed. Several measurements have been made on the strip under various conditions, to arrive at some reasonable estimate of the noise figure. A 5 Kc audio bandwidth was estimated, and the noise figure over theoretical noise appears to be 11 - 13 db under the several conditions of measurement, taken at this time only at room temperature.

### 3.4.5 Inclusion of Crystal Filter

Since the writing of the first part of this report, a 12 Mc crystal filter has been added between the generator element

and the strip input. This not only greatly improves the selectivity at 12 Mc, but also suppresses the image at 11.09 Mc, and a second spurious image due to a spurious resonance of the ceramic filter in the IF section.

It appears all of the ceramic elements tested have strong resonances at various other frequencies besides the 455 Kc desired resonance. In some cases, notably at a frequency around 135 Kc, the strengths of these resonant peaks are only 3 to 6 db down from the fundamental.

With the crystal filter as incorporated, all images and spurious signals appear to be at least 50 db down.

### 3.4.6 Conclusions

This 12 Mc IF strip, which is at least 65 to 70% composed of Functional Electronic Block Amplifier Circuits, has been designed into a demonstration form, both as an educational study and as a demonstration of the present Motorola state-of-the-art capability.

## 3.5 A Useful Application of the Parasitic Effects Inherent in a Silicon Monolithic Structure

### 3.5.1 Introduction

This section describes some new experimental applications of the collector to substrate parasitic capacitance in FEB integrated circuits.

Utilizing the variance of the capacitance of this junction with bias, interesting applications in frequency modulation and frequency tuning were obtained.

In a monolithic silicon block integrated circuit, specifically of the kind where the reversed diode type of isolation is built-in around the circuit functional elements, the parasitics take the form of capacitances and resistances. The capacitance is the natural result of the reversed bias diode, and the resistance is due to junction leakages. Both effects are well known and universal in semiconductor devices.

The capacitance associated with a transistor collector which is used as a signal amplifying output element is the most serious of the parasitics which couple all parts of the circuit to all other parts in some measure.

A transistor collector region is necessarily somewhat extended in area by the requirements of the structural geometry. Even the so-called small geometry transistors designed for high frequency applications have appreciable collector area.

The capacitance of the junction between the collector and the isolation area is on the order of 0.1 pfd per square mil. This means that such collectors will be loaded by shunt capacitances of 10 to perhaps 40 pfd in most useful small transistor geometries. One such situation is shown in Figure 6, in which A represents an NPN transistor immersed in the P-type substrate, and B, other circuit elements also immersed in the same conductivity medium.

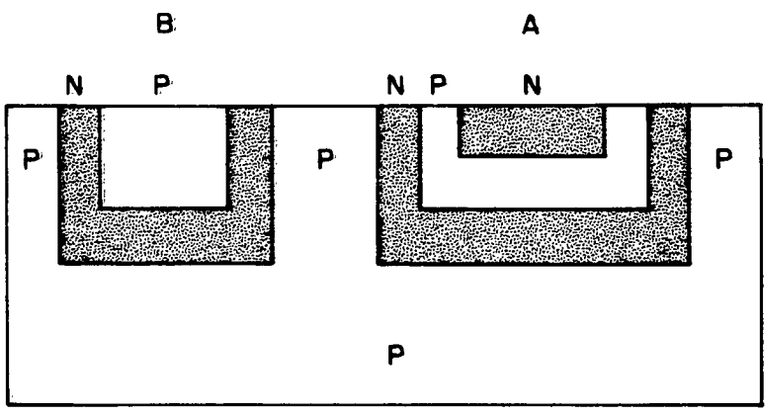



FIGURE 6

This capacitance appears in the circuit effectively as a shunt element Cp from collector to ground, such as shown in Figure 7.

It has been shown in another report how this Cp parasitic becomes deleterious in frequency limitations in RC coupled circuits, but becomes "tuned out" in inductively coupled circuits.

This report discusses some further extremely interesting effects in this isolation junction which give rise to some new operational functions, some of which can only be obtained as simply in monolithic silicon circuits.

### 3.5.2 Extraneous Reactions in the Isolation Junction

In all reverse biased semiconductor junctions, there is one factor which differentiates these from conventional capacitors. This is the voltage or bias sensitive capacitance effect. This is well known in special diode structures called varicaps.

In this sense, we have within the Functional Electronic Block built-in varicap actions, or voltage sensitive capacitances, which can be used to advantage in operational circuit systems.

This report describes some simple frequency modulation, trimmer tuning, and self biasing effects in an operating collector junction isolation diode, which may be harnessed to provide sometimes much simplified circuit functions.

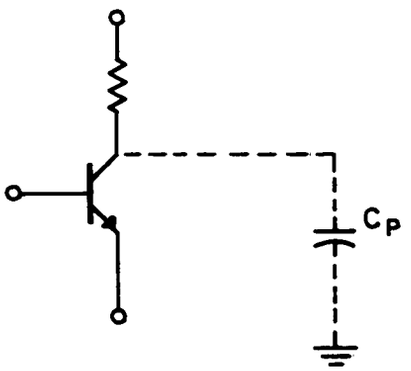



FIGURE 7

Two forms of FEB solid block amplifiers are shown in Figure 8, A and B. A is the Motorola emitter coupled configuration (MECA) and B, a more conventional grounded emitter amplifier. Both of these are shown with inductive loads and feedback circuits to produce sustained oscillations. These differ mainly only that in A, the MECA, the output and input are in phase, hence, the only feedback element required is a simple feedback capacitor $C_1$. In B, a conventional grounded emitter amplifier, the 180 degree phase reversal is obtained from a feedback coil $L_2$ or other suitable means.

In both of these circuits, the parasitic collector capacitance Cp becomes all of, or part of, the LC resonant load circuit.

Restricting the discussion now only to the isolation diode associated with the active output collector in both circuits, we see that the following effects can take place.

### 3.5.3 Junction Rectification

In the model of Figure 6, it is seen that the N collector immersed in the P substrate medium, provides under certain conditions, rectification of some of the signal on the collector. This is made more clear by reference to a highly over-simplified equivalent circuit of Figure 9. In this circuit, the inductive load is partly or wholly resonated by the isolation diode capacitance. Rectification at this diode on the negative swing, causes a small current $I_p$ to flow to the circuit ground through the parasitic reactances within the block.

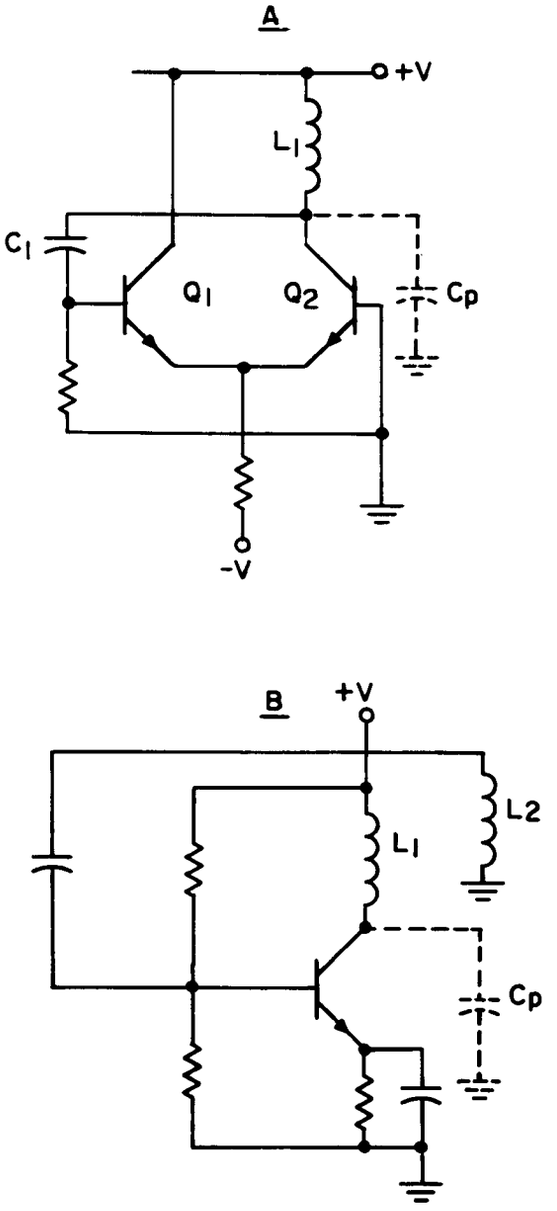



FIGURE 8

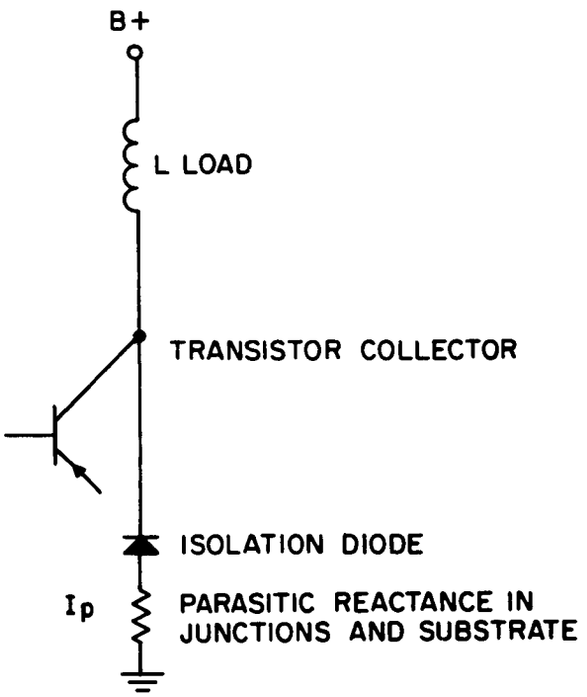

B+
L LOAD
TRANSISTOR COLLECTOR
ISOLATION DIODE
Ip
PARASITIC REACTANCE IN
JUNCTIONS AND SUBSTRATE

FIGURE 9

The RF drop across this path causes the substrate to raise somewhat positive, to some average D.C. value, above the circuit ground. This drift upward in potential occurs when the substrate is allowed to float. On the other hand, the substrate can be electrically tied to the circuit ground, whence this effect will not occur.

It is these two conditions, and those in between, in which the interests of this report are slanted.

### 3.5.4 The Built-in, Self-biased Varicap in the FEB

As we have seen, the collector isolation diode can provide inherently several functions of interest in certain applications. These are, (1) the self bias effect with floating or semi-floating substrate, and, (2) a $\Delta Cp$ which goes along with this bias. This almost immediately suggests a modulated FM oscillator or transmitter. (See Figure 10)

Under several experimental conditions, we have applied this effect to FM transmitters. Frequencies up to 45 Mc have been obtained with available FEB structures, and really very excellent voice and music reproduction by the simple expedient of applying almost any microphone, crystal or dynamic (1000 ohms impedance), directly between the FEB substrate and the circuit ground.

The FM signals were picked up on a Marconi AM-FM all wave receiver, with really very good fidelity in all cases. No attempts have been made as yet to measure or characterize the

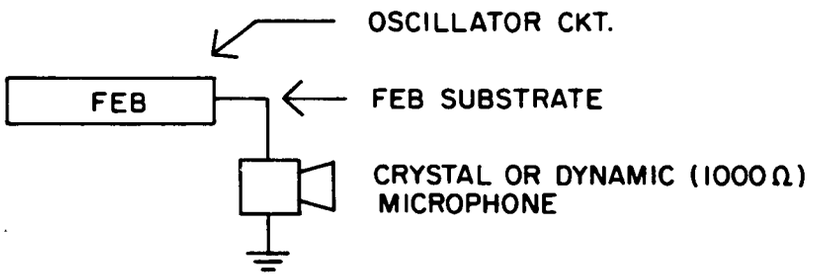

OSCILLATOR CKT.
FEB
FEB SUBSTRATE
CRYSTAL OR DYNAMIC (1000Ω)
MICROPHONE

FIGURE 10

many essential FM characteristics. The experiment appears to indicate that:

1. The inherent effect must be of effectively high impedance (crystal microphone).
2. No auxiliary modulator amplifiers are required.
3. The effective frequency modulation must be quite linear, as evidenced by the sound quality of all sound sources tested.

A low power FM oscillator can be designed in an extremely small space, which might be applicable in the areas of "micro FM" sensing devices.

One of the effective circuits used is shown in Figure 11. The FEB circuit, shown within the dotted lines, is entirely composed on a .100 inch square silicon block. This, and the other peripheral parts except the microphone and batteries occupy a space of less than .25 an $\overline{\text{inch}}^2$, $L_1$ is a sub-miniature 1 microhenry choke, $C_1$ 3 pfd feedback capacitor, $R_1$ 4.7K 1/10 watt resistor, $C_2$ and $C_3$ bypass capacitors, 470 pfd, and $B_1$, $B_2$, 1.5 volt miniature mercury batteries. The antenna is a straight wire 12" long, and the microphone a 1000 Ω dynamic hearing aid type. The frequency obtained in this set up was approximately 36 Mc, and the stability of the circuit was excellent.

In an oscillator circuit of similar nature to Figure 11, a miniature variable resistor between the substrate and the circuit ground provides stable frequency control, (Figure 12). One oscillator of this nature has been used as the local oscillator in a single sideband model receiver, completely built of

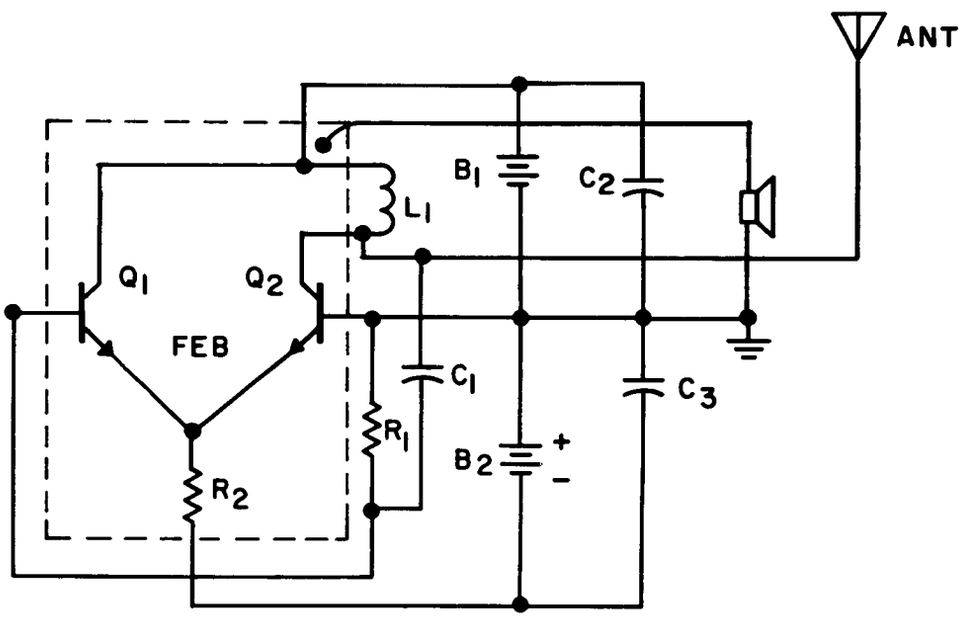



FIGURE II

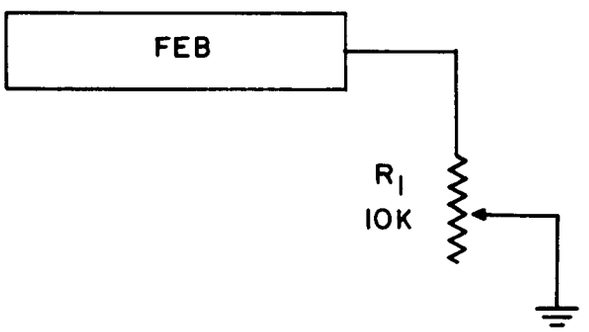



FIGURE 12

integrated circuit elements. This vehicle is the subject of section 3.6.

### 3.5.5 A FEB Design Example

In the circuit of Figure 11, and the very small FM transmitter which can be assembled from the FEB block and miniature peripheral components, the block itself is physically the smallest component. Further, there is room and capability for the inclusion of all of the circuit elements except the inductor on the block. High Q inductors cannot, at this time, be integrated in any block form.

If such a block were deliberately designed for a FM oscillator stage, the following design considerations would be employed:

1. Transistors $Q_1$ and $Q_2$, the latter especially, would be the smallest geometry, highest frequency units available for integrated circuits. This would provide for operational frequencies in the regular FM bands or above.

2. Resistors $R_1$ and $R_2$ could be diffused units as presently used in some designs, but there are indications that some observed leakage currents appearing in the present diffused blocks from the B+ system into $R_2$ could be eliminated by making $R_2$ a thin film compatible structure.

3. $C_2$ and $C_3$ are diffused units, each occupying about 30 x 40 mils of block surface.

4. $C_1$ could very readily be designed as an oxide capacitor directly over some portion of the base area of $Q_1$. This would require a modified $Q_1$ geometry somewhat as shown in Figure 14, in which A is the emitter area and contact, B the base contact, C a metalized area over the oxide to provide feedback capacitor $C_1$, and D the conventional collector contact.

For the required capacitance of 3 pfd, the area of the metalization B, at 0.1 pfd/mil$^2$, is about 30 mils$^2$. This could readily be accommodated on a slightly enlarged transistor geometry. Note that in the MECA circuit, the geometry of transistor $Q_1$, since it is an emitter follower, is less sensitive to frequency limitations than is $Q_2$.

### 3.5.6 Conclusions

This report has described some early experimental results in using the inherent parasitic effects encountered in FEB or monolithic silicon structures, to provide new or useful circuit functions.

## 3.6 The Design of an Integrated Circuit Pocket Size 4 Mc Single Sideband Receiver

### 3.6.1 Introduction

This design was undertaken as an experimental vehicle to demonstrate a concept which is probably quite important in systems design with integrated circuits. This concept is especially true in the application of Functional Electronic Block Circuits to a system.

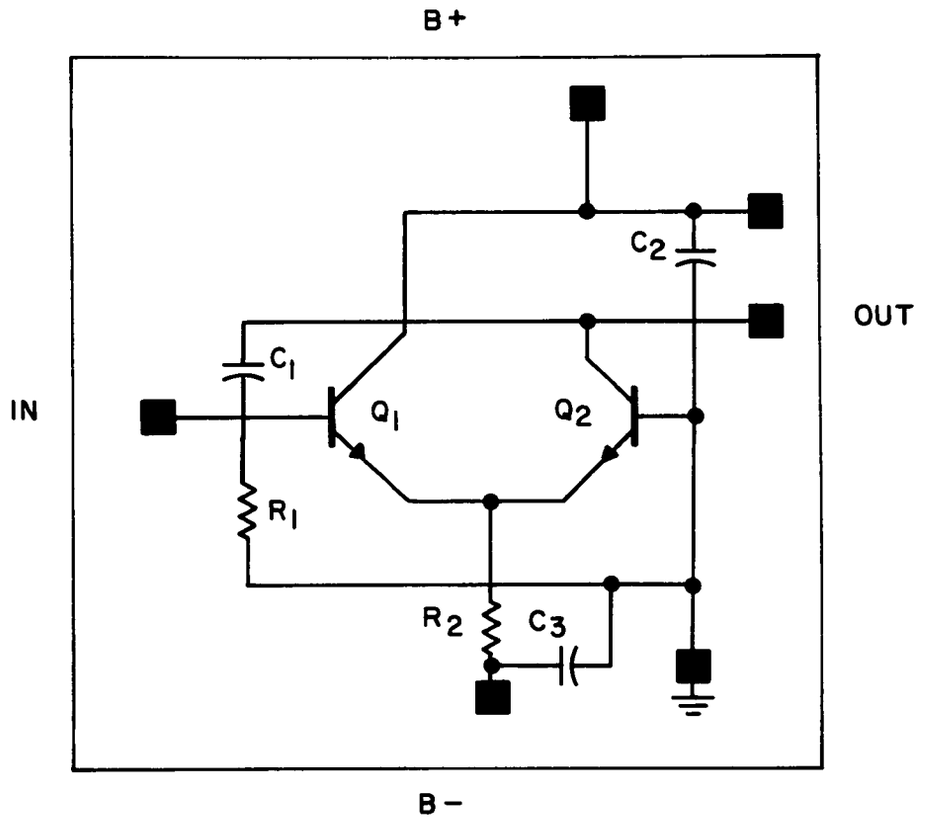



FIGURE 13

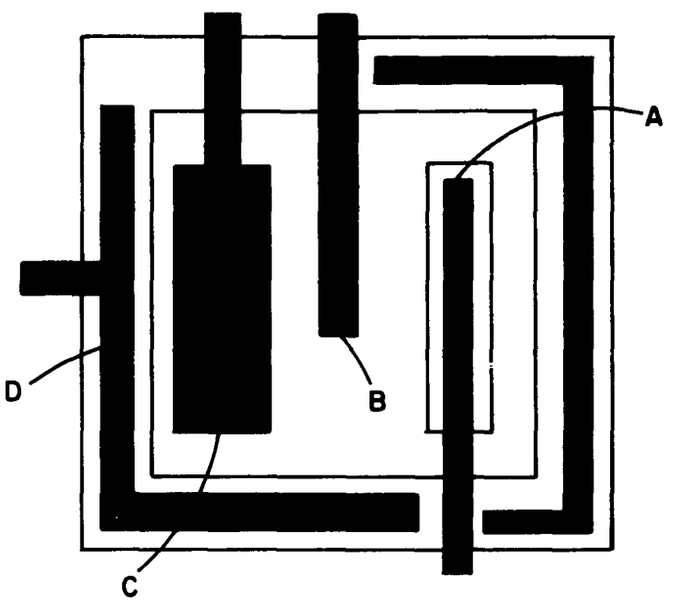



FIGURE 14

Since FEB circuits represent a considerable investment in design time and effort, it is expedient, within this concept, to use the same circuit in as many places as possible in the system, even though the performance on a stage by stage basis may not be as optimized as could be achieved with conventional circuit methods. This obviously reduces the number of different circuit configurations required for a given system. In the system described in this report, which is a high sensitivity special purpose receiver, this design philosophy was followed, resulting in a system with excellent performance in which the same basic circuit is used for all functions except one.

Further, the amplifier circuit adopted is very amenable to FEB fabrication. Some FEB versions of this amplifier are presently being completed and will be ready for evaluation in a few weeks. Also, some FEB MECL gates, which also form the basic amplifier part of this circuit have been evaluated in several positions in this receiver.

The receiver models have been constructed so far with Hybrid Integrated Circuits in TO-5 cans. In one of the incompleted models, a MECL FEB amplifier is used to provide an interesting frequency variable oscillator for the carrier reinjection in the single sideband product detector.

### 3.6.2 Basic Amplifier and Circuit Configurations

The emitter coupled RF amplifier has certain advantages for FEB fabrication over the more conventional grounded emitter configurations generally used in linear systems design. These prime advantages are:

1. Inherently stable and non-critical circuit.
2. Because of the Beta C multiplying effect, bypass capacitors when used are much smaller in value even at the lower frequencies than equivalent capacitors required in the grounded emitter configuration.
3. These capacitors can readily be included on a reasonably sized FEB block.

The basic two-transistor emitter coupled amplifier is shown in Figure 15. This is the basic configuration adapted for use in this receiver vehicle. This is used in three slightly different versions.

In all of these, the power supply is split with a + level with respect to ground on the collector leg, and a - level, with respect to ground, on the emitter leg. A variation in this - voltage level varies the stage gain and, therefore, performs an AGC or sensitivity level control.

This type of operation requires no bypass capacitors whatever. In another version, adapted for a single supply (Figure 16), the bypass capacitor $C_1$ of approximately 450 pfd is adequate for frequencies of 455 Kc and above.

The three circuits shown in Figure 15 can all be derived from a common FEB block with different metalization masks.

Version A is used for RC coupled voltage amplifiers, such as the 455 Kc stages and the audio pre-amplifier in the experimental vehicle.

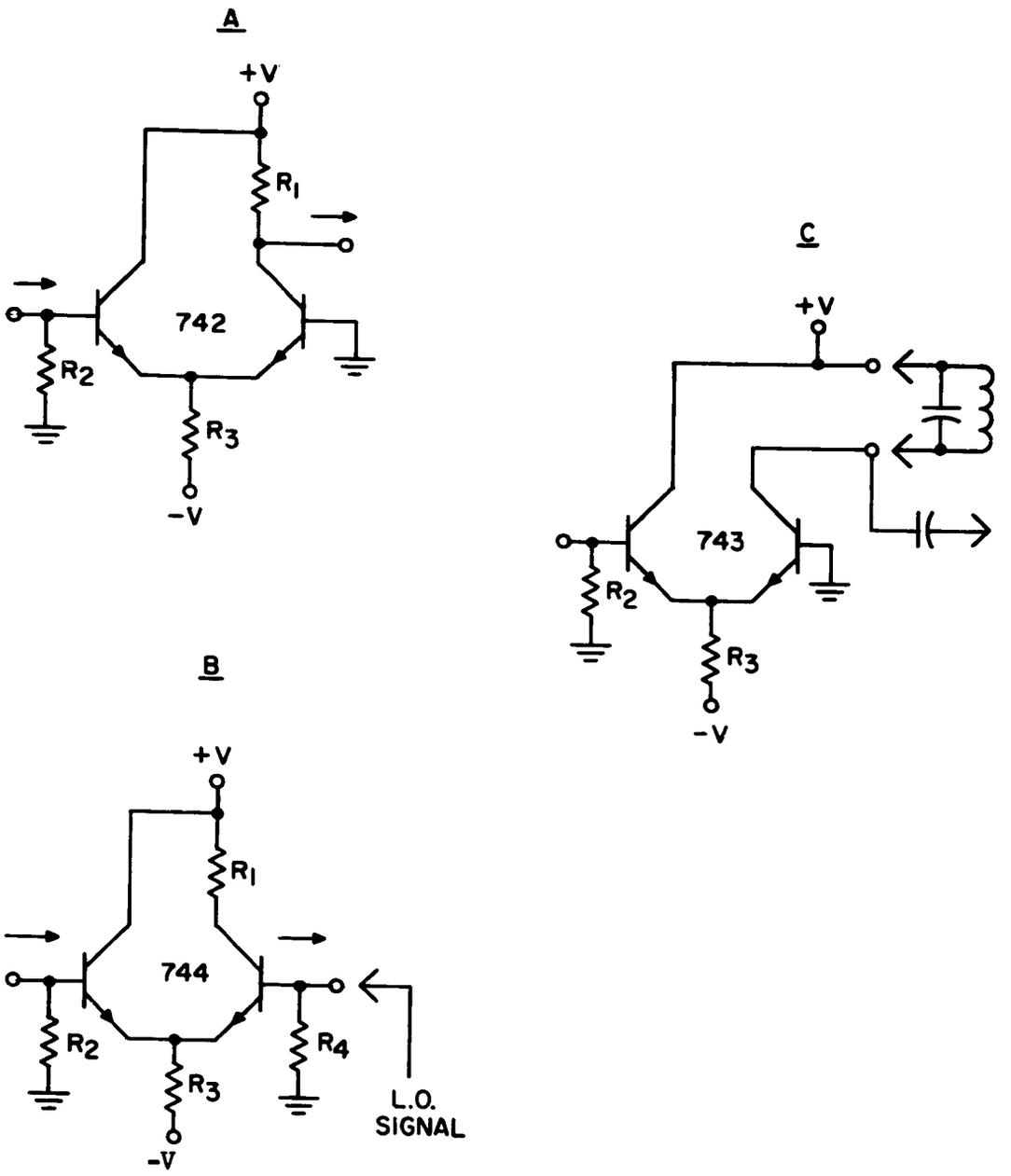



FIGURE 15

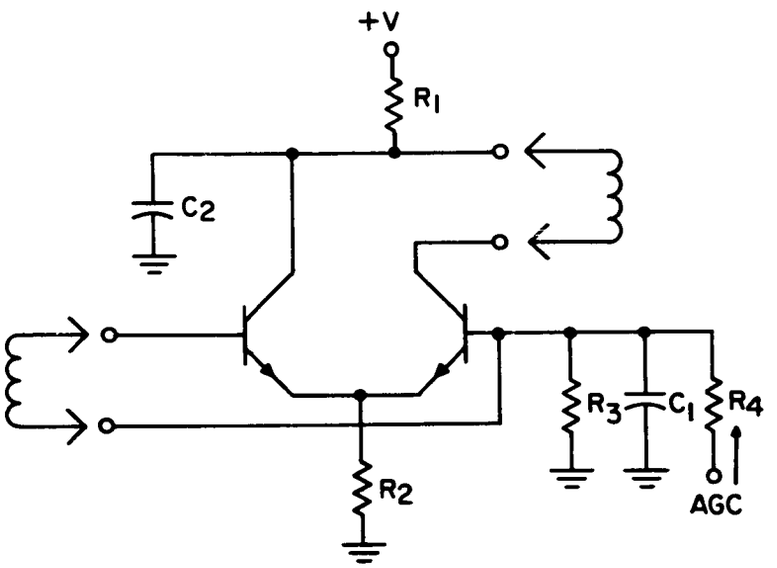



FIGURE 16

Version B simply adds a second resistor to $R_4$ for the injection of a local oscillator signal. This stage is used for a mixer or product detector application.

Version C differs from A only in the omission of the load resistor $R_1$. This stage is used with external inductive elements for the RF amplifier and the LC coupled local oscillator applications.

### 3.6.3 Receiver Layout and Stage Functions

A block functional diagram of the 4 Mc S.S.B. receiver is shown in Figure 17. The blocks numbered 742, 743, etc., refer to the configurations of the emitter coupled RF amplifier as detailed in Figure 16 preceding.

The antenna stage $S_1$ consists of an RF amplifier with tuned 4 Mc loopstick antenna $L_1$. This is provided with an aperiodic winding $L_2$ connected to a jack for an auxiliary throwout wire antenna when more sensitivity is required. The collector output of the 743 stage is loaded with a miniature slug tuned choke and resonating capacitance, also tuned to 4 Mc.

This is coupled to the 744 mixer stage, $S_2$, which also receives a signal from the 4.455 Mc local oscillator, $S_9$. $S_9$ is a crystal controlled configuration oscillating in the crystal fundamental mode, 4.455 Mc. A schematic of this stage is shown in Figure 18.

The mixer output is coupled to the first IF stage $S_3$ (742). through a frequency resonant ceramic filter element $C_{R_1}$.

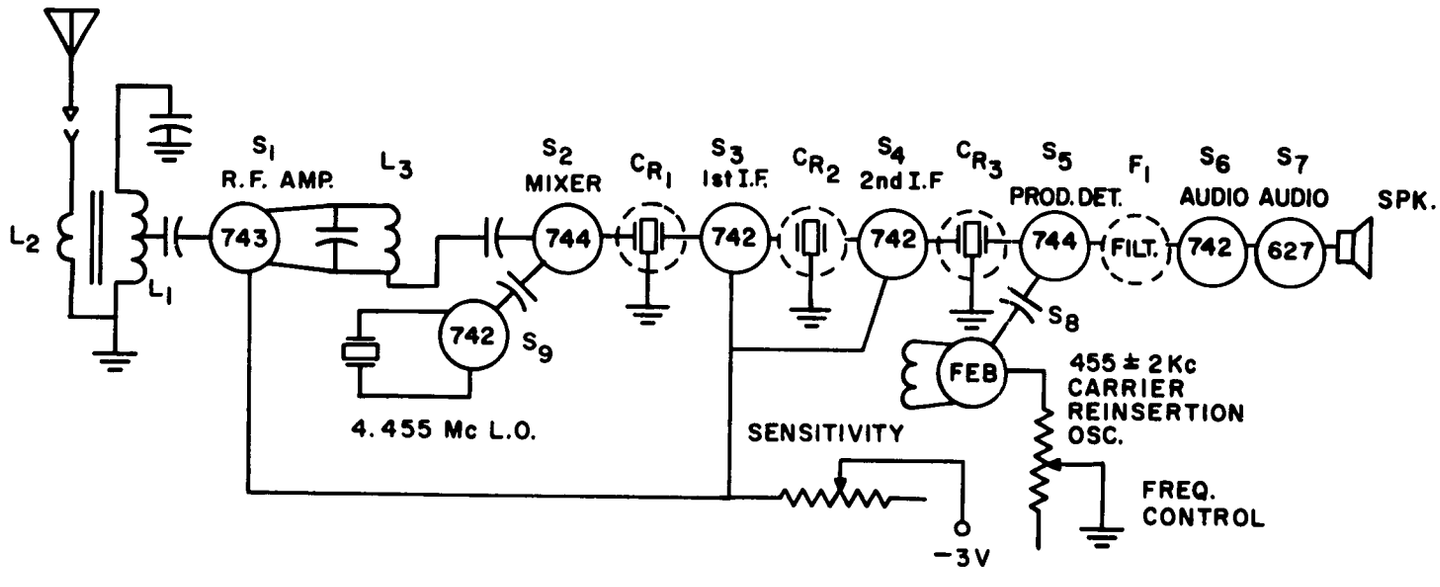
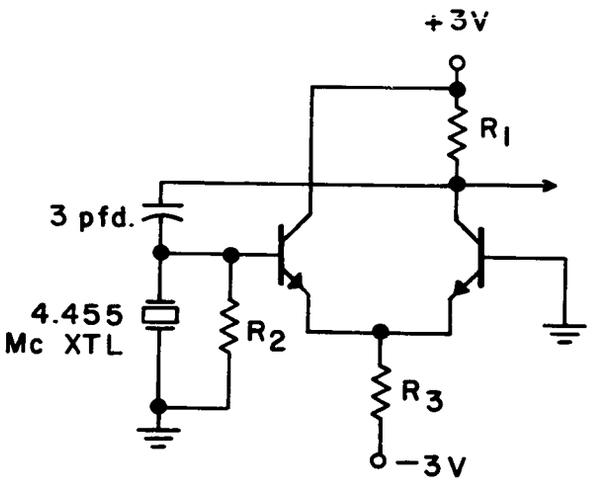

L2
L1
743
S1
R.F. AMP.
L3
S2
MIXER
744
CR1
S3
1st I.F.
742
CR2
S4
2nd I.F
742
CR3
S5
PROD. DET.
744
F1
FILT.
S6
AUDIO
742
S7
AUDIO
627
SPK.
742
S9
4.455 Mc L.O.
S8
FEB
455 ± 2 Kc
CARRIER
REINSERTION
OSC.
SENSITIVITY
FREQ.
CONTROL
-3V

FIGURE 17




4.455 Mc LOCAL OSC.

FIGURE 18

A like coupling is used between $S_3$ and the second IF stage, $S_4$ with $C_{R_2}$. A third ceramic element $C_{R_3}$ couples the IF output into the product detector, $S_5$. These ceramic filters are mounted in individual TO-5 packages for uniformity with the other TO-5 packaged circuits.

The product detector $S_5$ (744) is fed on its second base input with a 455 Kc $\pm$ 2 Kc signal from the local oscillator $S_8$. This reinserts a properly oriented 455 Kc carrier into the single sideband signal, providing undistorted demodulation. The $S_9$ stage is a special and novel FEB application more fully described in another part of this report.

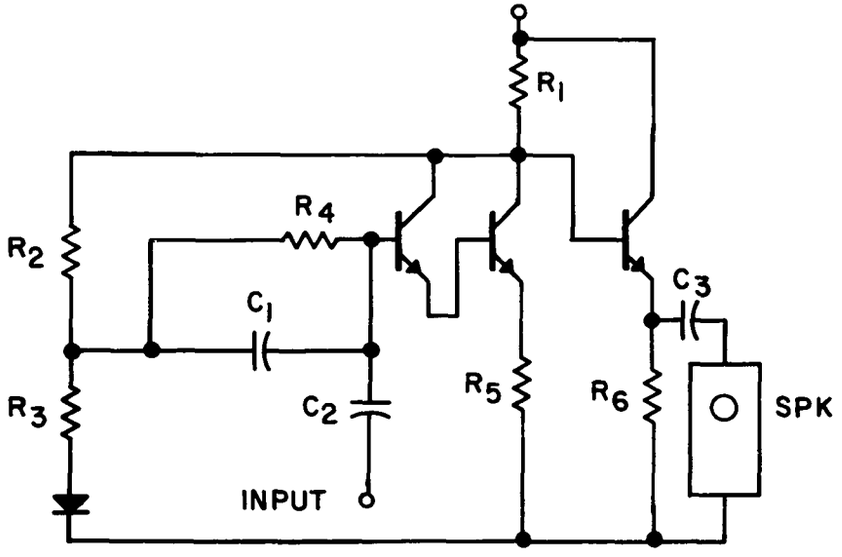
The product detector output passes through a low pass two section RF filter, $F_1$ and into the first audio amplifier $S_6$ (742).

The output of $S_6$ goes into the final audio amplifier $S_7$. $S_7$ is the only hybrid integrated circuit structure (See Figure 19 for schematic) that is not based on the emitter coupled amplifier configuration.

Receiver gain control is obtained from a miniature variable resistor in series with the -3 volt supply source and the emitter control terminals of $S_1$, $S_3$, $S_4$, and $S_5$. Approximately 50 db of attenuation control is available.

### 3.6.4 The Special Carrier Injection Oscillator Stage

There are many ways in which the requirements of the carrier injection oscillator S8 may be provided. This oscillator must be stable to within a hundred cycles or so at any setting,




AUDIO OUTPUT AMPLIFIER

FIGURE 19

and be variable in frequence over a short range, such as $\pm$ 2 Kc. Its median frequency must be 455 Kc. The required output of the stage is not critical, but should be at least 2 volts P-P or more.

During the design of this receiver, several oscillator forms were evaluated. These ranged from the ordinary LC Hartley type feedback configurations, to some special Pierce configurations. One interesting Pierce version is as shown in Figure 20. This is an ordinary grounded emitter amplifier stage with a resistive load $R_1$ and a variable base bias through control $R_2$. The collector to base feedback is a ceramic resonant filter element $C_R$ identical to those used in the IF strip. Capacitors on the input and output elements provide a time constant consistent with the frequency. This oscillator is very stable, and may be warped across a range of frequencies of $\pm$ 3 Kc from the nominal 455 Kc by varying the control $R_2$. This oscillator was used with satisfactory results in one of the SSB models.

A very simple oscillator circuit is provided from a 742 emitter coupled amplifier, as shown in Figure 21. This circuit oscillates from the simple series resistor-capacitor coupling between collector and input because of the in phase relationship of these elements in this particular amplifier. A very wide range of frequency and control range may be obtained by selecting suitable values of $C_1$ and $R_2$. This oscillator, though interesting, was not considered stable enough for the SSB receiver use.

The very interesting circuit shown in Figure 22 imparts a flavor of novelty, since it involves an inherent circuit function only available in an FEB block circuit. It will not control the

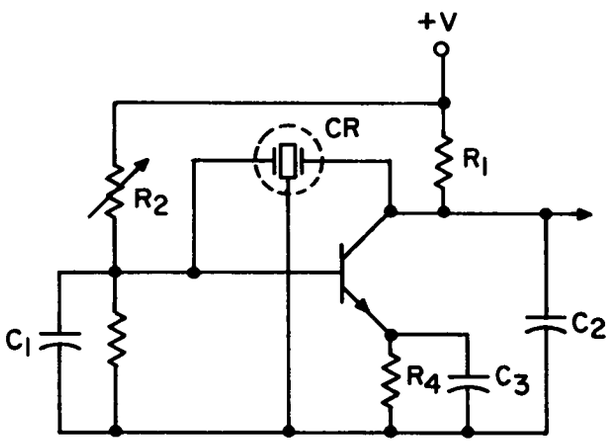



FIGURE 20

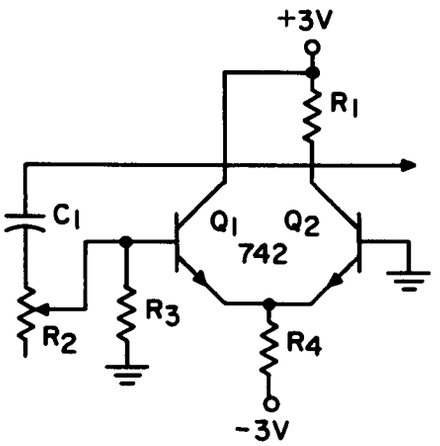



FIGURE 21

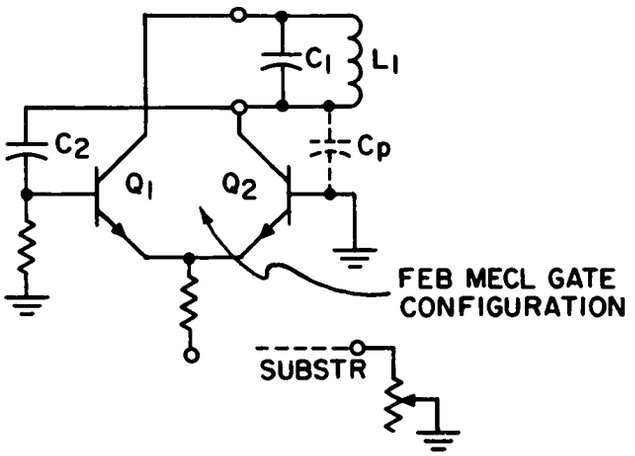



FIGURE 22

frequency by this means in either a conventional or a hybrid integrated circuit. The circuit is based on an FEB version of the emitter coupled amplifier as derived from a MECL gate structure. In the MECL gate, as in the FEB versions of the coupled amplifier, both transistor as well as the emitter resistor $R_3$ are diffused into the silicon block.

The output collector is provided with tuned choke $L_1$, and $C_2$ provides the in-phase positive feedback to sustain oscillations. $L_1$ is resonated to 455 Kc with a fixed capacitor $C_1$ and the inherent collector to substrate capacitance $C_p$ due to the isolation diode under the collector of $Q_2$.

$C_p$ is a function of the reverse biased isolation diode, and in common with all such diodes, the capacitance changes with voltage bias. This is the familiar varicap effect.

A highly simplified equivalent circuit of this situation is shown in Figure 23, in which $X_L$ represents the load reactance, C the transistor collector, $C_p$ the isolation diode, and $X_R$, $X_C$ some resistive and capacitative reactances within the block substrate. As the oscillatory voltage on C moves up and down, there is some current rectification across the diode $C_p$ on the negative voltage swings. This results in a small current flow through $X_R$ $X_C$ which are resultant load reactances throughout the block due to circuit parasitics.

This results in the substrate tending to assume a positive bias with respect to the circuit ground when it is allowed to float, and results in a somewhat smaller total resonant capacitance ($C_1$ + $C_p$, Figure 22) than when the substrate is shunted to ground.

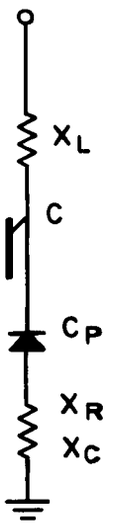



FIGURE 23

Thus, a simple variable resistor between the FEB substrate and ground (Figure 24) provides a smooth frequency control between these limits.

It is possible to obtain quite substantial frequency trimming by this method by properly apportioning the resonant L and $C_1$ values with respect to the effective $\Delta C_p$. This oscillator is quite voltage sensitive, but with a stabilized supply level such as by zener diode control, a very stable oscillator, apparently quite free from drifting is provided.

A more informative review of this phenomenon, as well as other applications, such as FM modulation, will be discussed in following reports.

This oscillator configuration is not claimed at this time to be any better than other possible oscillators for this SSB application, but it certainly is an example of the utilization of a phenomenon which exists in, and can only be reproduced by, FEB structures of the isolation diode type.

### 3.6.5 Packaging Problems

As far as the electronics part of the integrated circuitry developed in this vehicle, the performance appears quite good in both breadboard and HIC models. The actual SSB sensitivity could not be measured directly, due to lack of calibrated equipment at this time, but has been estimated at about -95 to 100 D.B.M. for a threshold audible signal.

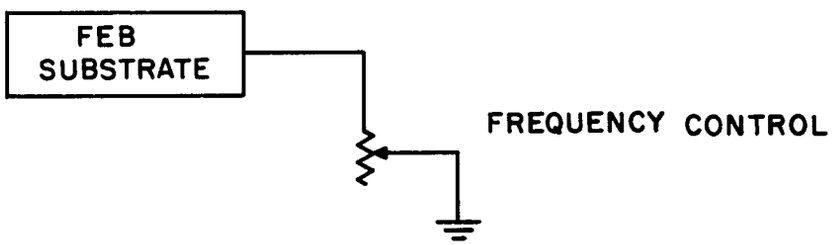



FIGURE 24

The rather uncommon design approach - that of using a common circuit form for all functions is somewhat novel, and appears to be the preferred integrated circuit approach to integrated circuit systems design.

Several problems remain in placing this circuitry, along with the required peripheral equipments, into the selected receiver package. It is at this time a "just merely make it" situation, which by the very closeness of the related circuit components, has lead to feedback and regeneration effects which may require a considerable time to neutralize.

Therefore, at this time, the development has been considered effective as a design exercise only. It is felt that considerable groundwork has been laid in establishing design approaches with the forthcoming FEB circuits for linear applications. It is believed further that this exercise has helped establish some new ground rules in the application of FEB integrated circuitry that will be useful in the fields of communications and other developments to come in the general area of FEB linear circuitry.

## 4.0 PACKAGING AND INTERCONNECTIONS

### 4.1 Experimental Interconnection Methods

The techniques of obtaining a stable interconnection between the Al metalization of the die and the feed-through, presents many problems. The more recent use of ultrasonic Al wire bonds has enhanced the possibility of a stable bond to the feed-throughs of the TO-5 header presents other problems, such as adhesion, plating and stability during the actual bond.

Recent experiments with a Kovar contact plate (Figure 1) show promise. Al metal is evaporated on the die contact side at 550°C. The other side of the contact plate is used for securing a solderable contact to the feed-throughs using AuGe solder. After soldering to the feed-throughs, the outer support ring of the contact plate is removed and an ultrasonic bond is made to the die. Thorough test data are not available as of this time.

Solderable contacts are also being investigated. The use of AlGe as a solder for bonding the contact plate to the Al metalization of the die exhibits good possibilities (Figure 2). The eutectic AlGe is deposited on the bonding areas of the contact plate by evaporation (Figure 3).

Problems that exist, at present, in the 424°C AlGe system appear to be in the deposition of Al and Ge in the proper amounts so as to prevent the Al metalization of the die from being dissolved by the AlGe solder (Figure 4).

FIGURE 1
Kovar Contact Plate

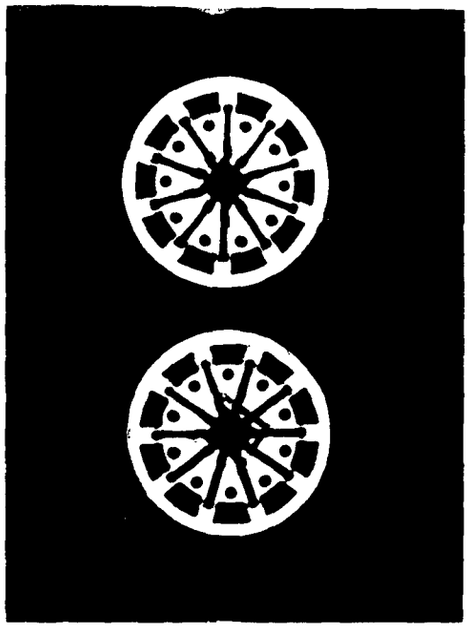


FIGURE 2
AlGe Solder Bonding

FIGURE 3
Evaporation of AlGe Solder

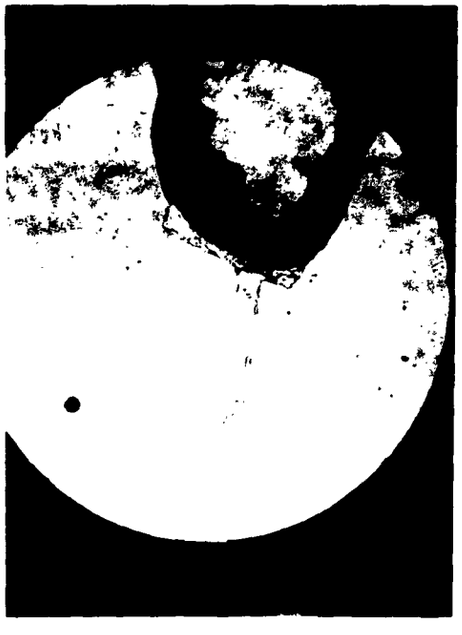


FIGURE 4
AlGe Aluminum Solder Bonding

## 4.2 Flat Package Development

Package development has been completed for Monolithic Circuits. Interconnections can be achieved either by existing wire bonding techniques or an extension of the feed-throughs for the more recent "finger" method.

This one-fourth inch square flat package, as shown in Figure 5, which has five leads extruding from two opposite sides, is approximately fifty thousandths of an inch thick. A complete package has only four basic components, common to all of the prior mentioned types.

The bottom, which is the same part as the cover, (Figure 6) is a one-fourth inch square ceramic, ten thousandths of an inch thick. The sides are composed of a glass frame, having serrations allowing for the feedthroughs, (See Figure 7 and 8). The five thousandths thick kovar feed-through frame has an extension to provide for the finger contact to the silicon, (See Figures 9 and 10). In addition, this frame has holes necessary for alignment and stability during fabrication. The glass frit is applied to both the glass frame and the ceramic bottom. In the case of the finger method, the die is positioned on the bottom at this time also. The properly metalized feed-through plate is positioned between the bottom and the glass frame, (See Figure 11). In the wire bonded package, the frit is applied to this three-pieced assembly providing for the die bond to the ceramic bottom.

This assembly is heated in a belt fed furnace at 440°C, with an oxidizing atmosphere for approximately thirty minutes.

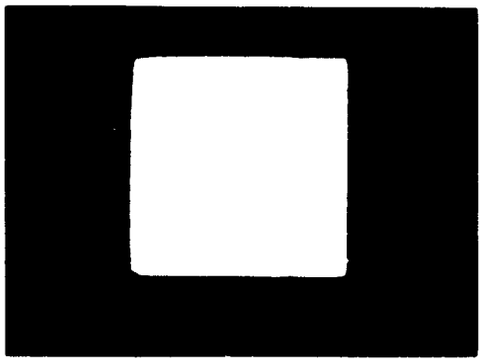


Figure 5

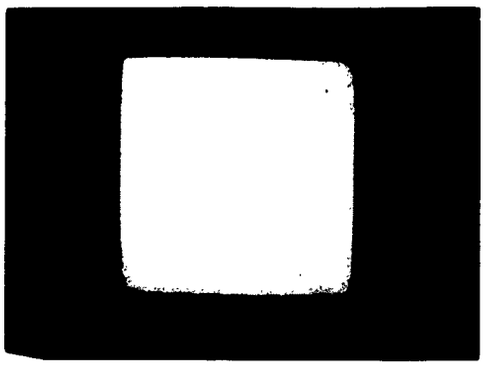


Figure 6

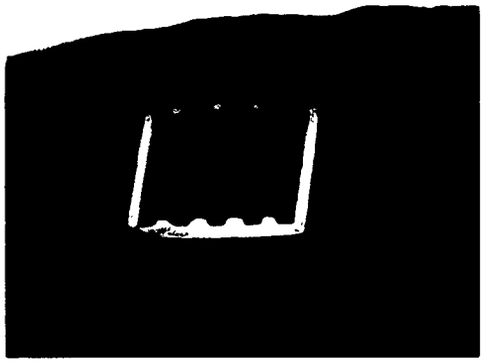


Figure 7

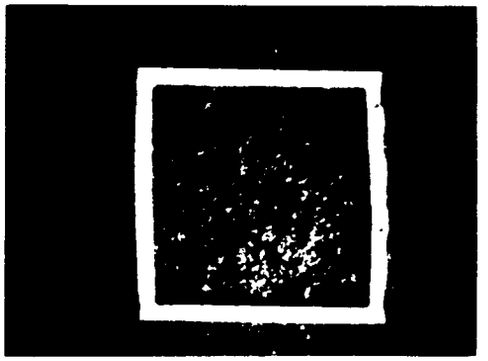


Figure 8

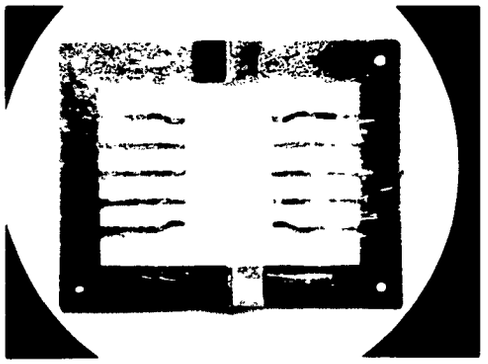


Figure 9

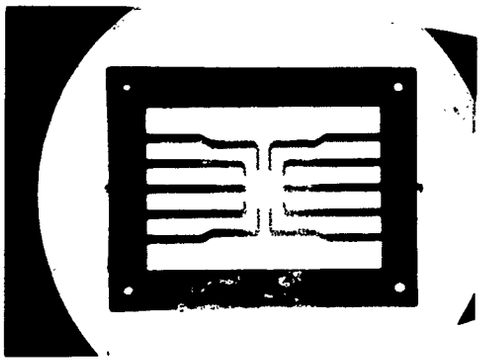


Figure 10

Necessary interconnection functions and testing, are performed prior to sealing the ceramic lid with the frit and second heating, (See Figures 12 and 13). The second heating is done at approximately 425°C; other conditions remain the same as in the prior heating (See Figure 14).

Various experiments in progress, at the present time, are hermetic sealing capabilities, strength testing of feed-throughs, internal and external metalizing of the kovar feed-throughs and thermal shock testing of this package. Reliability data, indicating the quality of this package, should be available soon.

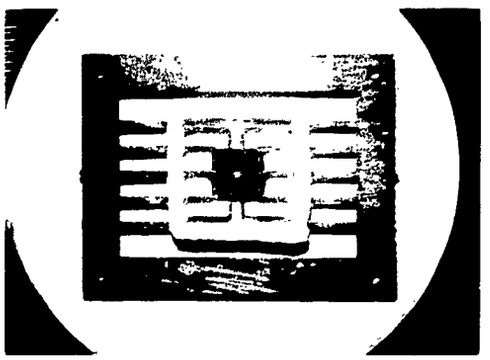


Figure 11

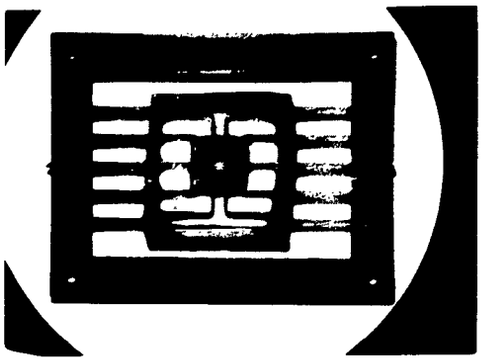


Figure 12

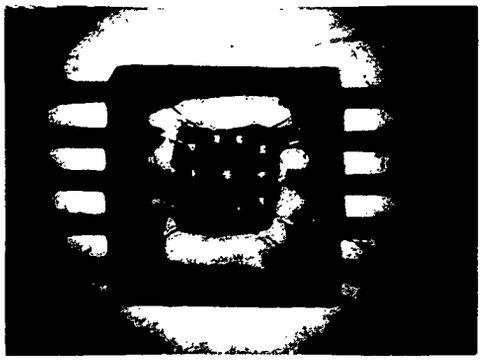


Figure 13

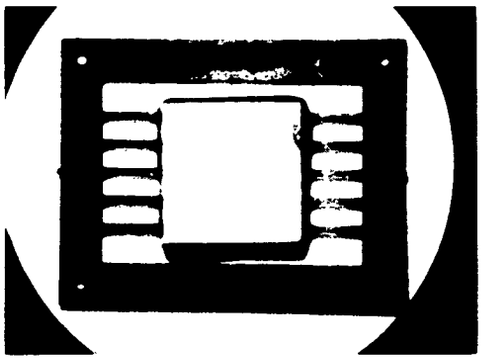


Figure 14

## 5.0 DIGITAL COMMUNICATIONS SYSTEM

### 5.1 Description of Digital Communication System

The basic system designed is a multi-channel voice-digital communication link. As a system, the unit will provide the capability for simultaneous transmission of several voice channels over a single wire. This capability is provided by the use of digital multiplexing techniques. In operation, each voice signal is sequentially converted into a binary representation at the transmitting terminal and converted back into voice signals (decoded) at the receiving terminal.

Figure 1 is a functional block diagram of the proposed system. The upper portion of the figure is the transmitting terminal and the lower portion is the receiving terminal.

Conditioning amplifiers are provided to suitably amplify the low level voice signals and provide a proper impedance level to the Multiplexer Unit.

The Multiplexer performs the function of sequentially connecting each of the three voice channels to the Digitizer. Each voice channel is connected to the Digitizer 8000 times per second.

The Digitizer will convert each voice sample into a 7-bit digital data word, thereby, providing amplitude resolution of better than one percent. This degree of resolution is more than adequate for reproduction of voice.

MULTICHANNEL DIGITAL VOICE COMMUNICATION SYSTEM

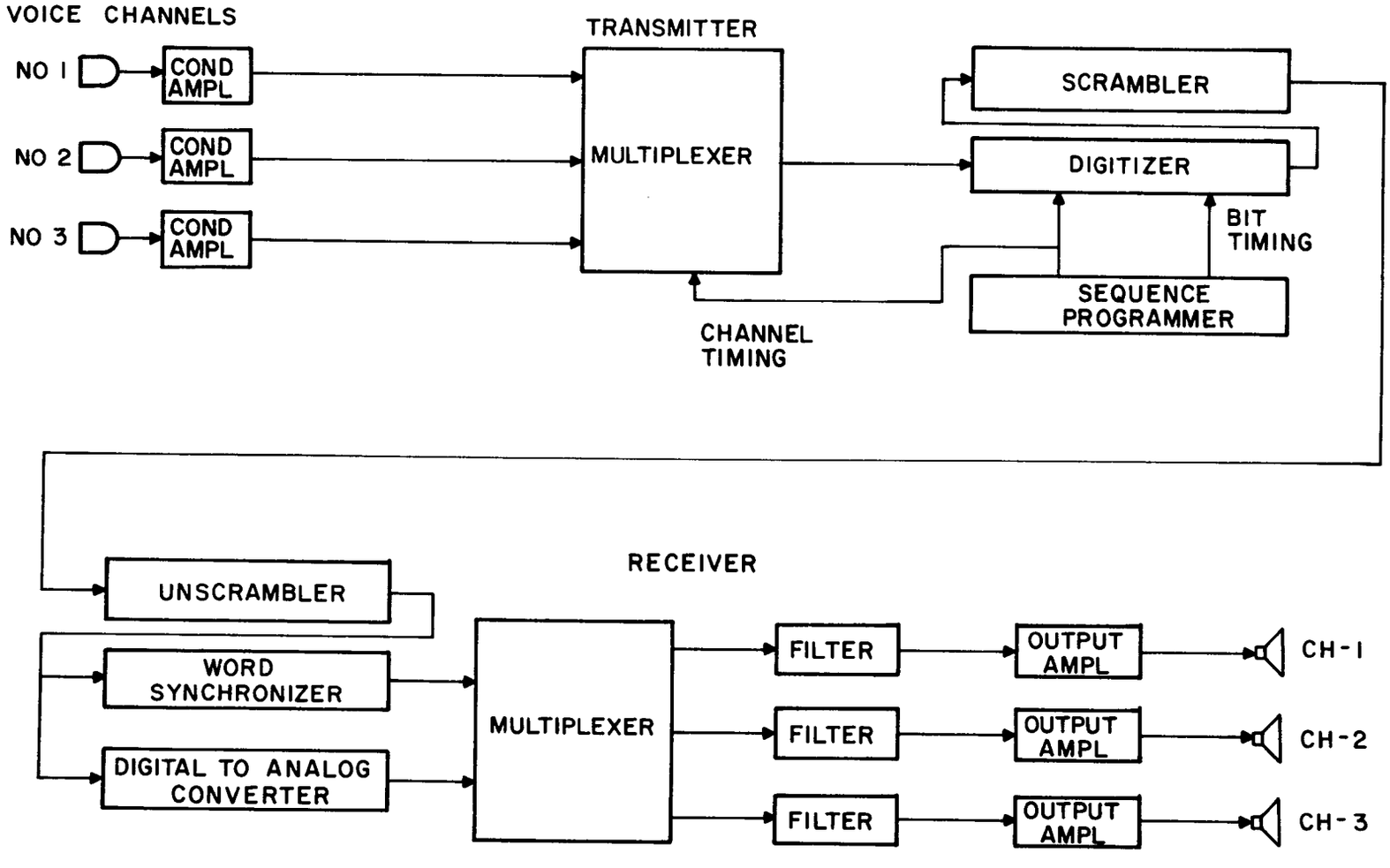



FIGURE 1

The Scrambler Unit has been included to demonstrate secure communications characteristics of digital communication links. A simple method of providing secure data in contrast to more sophisticated approaches has been selected. The secure aspects are realized by scrambling the digital words in a pseudo random fashion such that it is not possible to decode the data without knowledge of the exact scrambling code. The output of the transmitting terminal is the scrambled serial digital data.

The sequence timer provides the pulses necessary for performing the various timing functions in the transmitting terminal.

The receiving terminal performs the complimentary functions necessary to recover the original data.

The first operation which must be performed is that of deciphering the scrambled data. This is accomplished in the Unscrambler by prior knowledge of the scrambling code.

The word synchronizer provides proper channel identification for each word in a serial bit stream.

The Digital to Analog Converter accepts 7-bit serial words from the Unscrambler Unit and converts them to voice signals.

The Multiplexer serves to connect the Digital to Analog Converter Output sequentially to the proper channel outputs in a manner analogous to the multiplexing function at the transmitting terminal.

Suitable amplification and filtering are provided in each channel output.

The end result of the system will be three independent microphone inputs at the transmitting terminal, a wire coupling between the transmitting and receiving terminals and three independent loud speakers at the receiving terminal.

The system is an excellent vehicle for demonstrating the capabilities of integrated circuitry for a number of reasons.

1) The system can be demonstrated without requiring additional instrumentation.

2) Although the complete system does not necessarily have an operational application, the various elements comprising the system will find direct application to numerous digital communciation links.

3) The system requires the application of both linear and digital circuits.

4) Maximum utilization of previous contract work is realizable.

5) The number of new integrated circuit designs necessary to complete the system is small enough to fit into a realistic time schedule.

6) The system lends itself to being configured in modular form thereby permitting the integration of circuits and packaging on a functional subsystem basis. This permits the fabrication of functional and demonstratable units prior to completion of the total system.

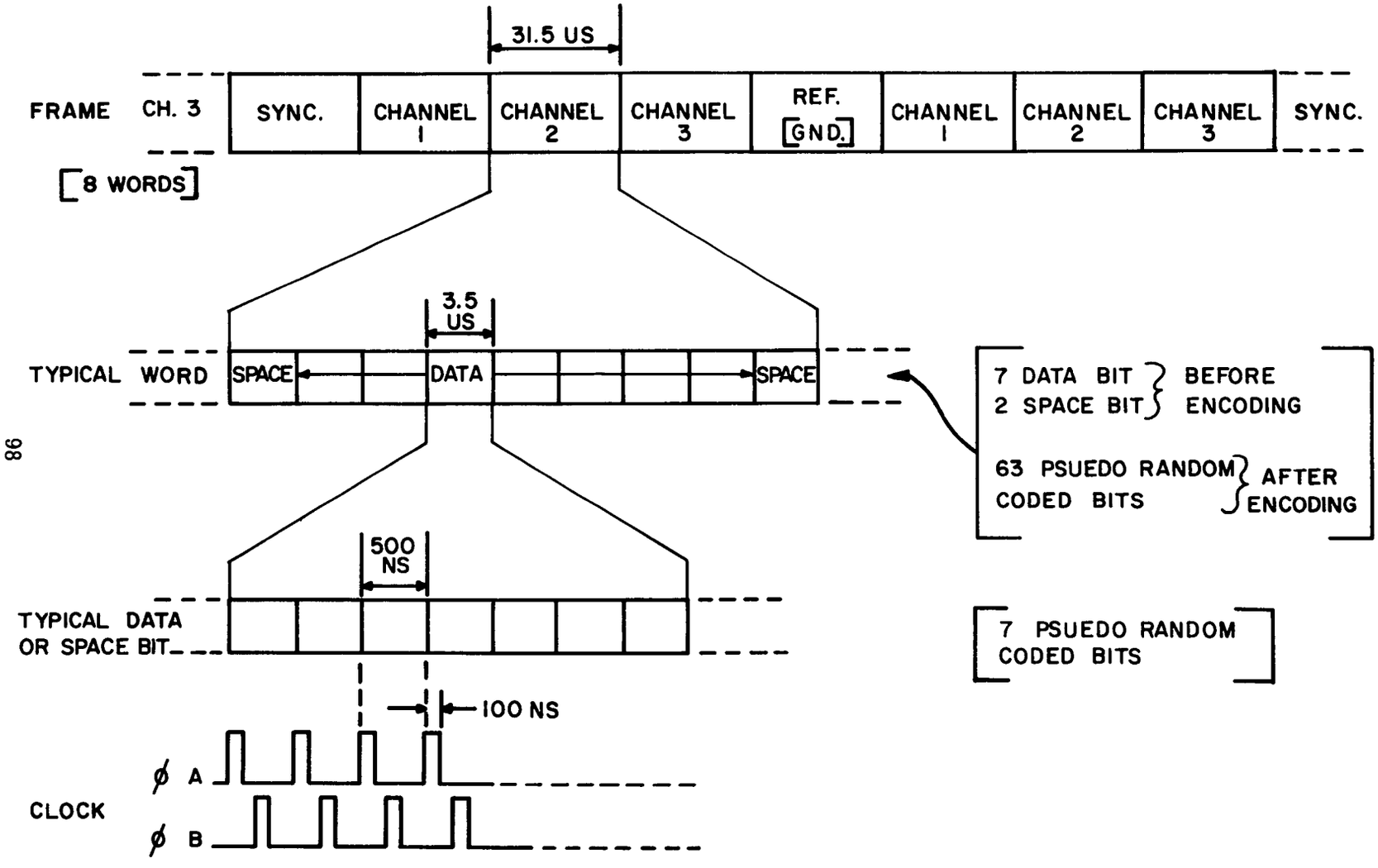
7) Implementation of the system does not require an excessive number of different integrated circuit types.

It is not necessary to fabricate in integrated circuits both transmitting and receiving terminals in order to provide a successful demonstration. It is conceivable that only the transmitting terminal will utilize integrated circuitry. However, it is significant that integration of the receiving terminal circuits require only a small number of integrated circuit types in addition to those used in the transmitting terminal.

## 5.2 System Operational Characteristics

The following system operational characteristics were established and provide the basis for the logic design for the breadboard system. The message format is shown in Figure 2.

1) Voice word rate - 8 Kc
   Synchronization word rate - 4 Kc
   Reference word rate - 4 Kc
2) The space bits will all be "zeros" (except for the sync word)
3) All data and space bits for the sync word (before pseudo random coding) will be "ones"
4) The pseudo random bit sync at the receiver is by wire (same oscillator)
5) The receiver will recognize sync upon determining that all 9 data and space bits of the sync word are "ones". A "one" for each of these bits is established when 6 out of 7 of the received code bits correspond with the local transmitter pseudo random code bits.




TRANSMITTED MESSAGE FORMAT

FIGURE 2

## 5.3 Comparator and Isolation Amplifier Design

Effort on these amplifiers has been consolidated in order to further investigate a common building block linear amplifier design. At present, the cascadable NPN differential stage and PNP differential stage still appears to be the most suitable. The NPN differential stage was tested using discrete components, including non-gold-doped-matched 2N834's. The following data was obtained.

| | Expected Single Chip Performance | Actual Non-Gold-Doped 2N834 Performance |
|---|---|---|
| Gain (single ended) | 4.6 | 4.0 |
| Bandwidth | 1 Mc | 3 Mc |
| Offset (referred to input) | 50 mV | < 1 mV |
| Common Mode Rejection | 40 db | 80 db |

These tests will be repeated using integrated circuit transistors as soon as they are available. A preliminary mask layout on the NPN stage was made indicating the component density is compatible with substrate area.

## 5.4 Multiplexer Switch Design

The function of the multiplexer switch in the system is to sample the audio signal at the output of the condition amplifier as shown in Figure 3.

The switch requirements to perform the system multiplexing functions at the 8 Kc sampling rate in the 31.5 μS sampling times are:

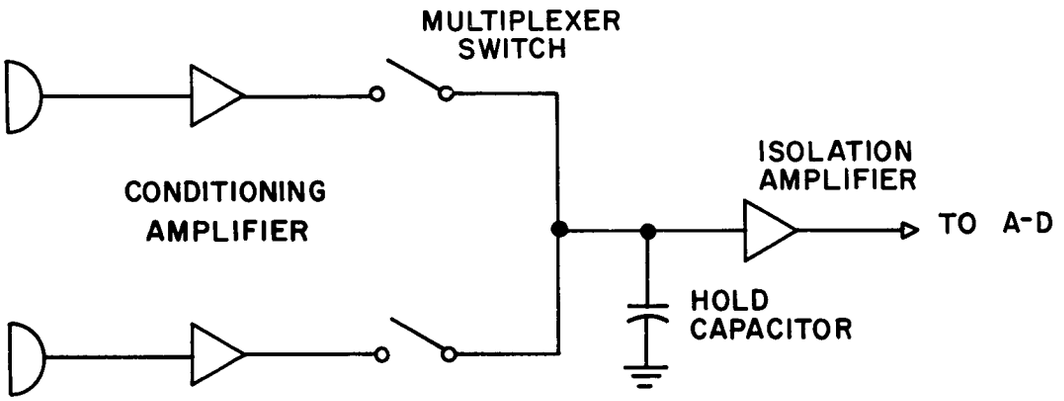

MULTIPLEXER
SWITCH
ISOLATION
AMPLIFIER
CONDITIONING
AMPLIFIER
TO A-D
HOLD
CAPACITOR

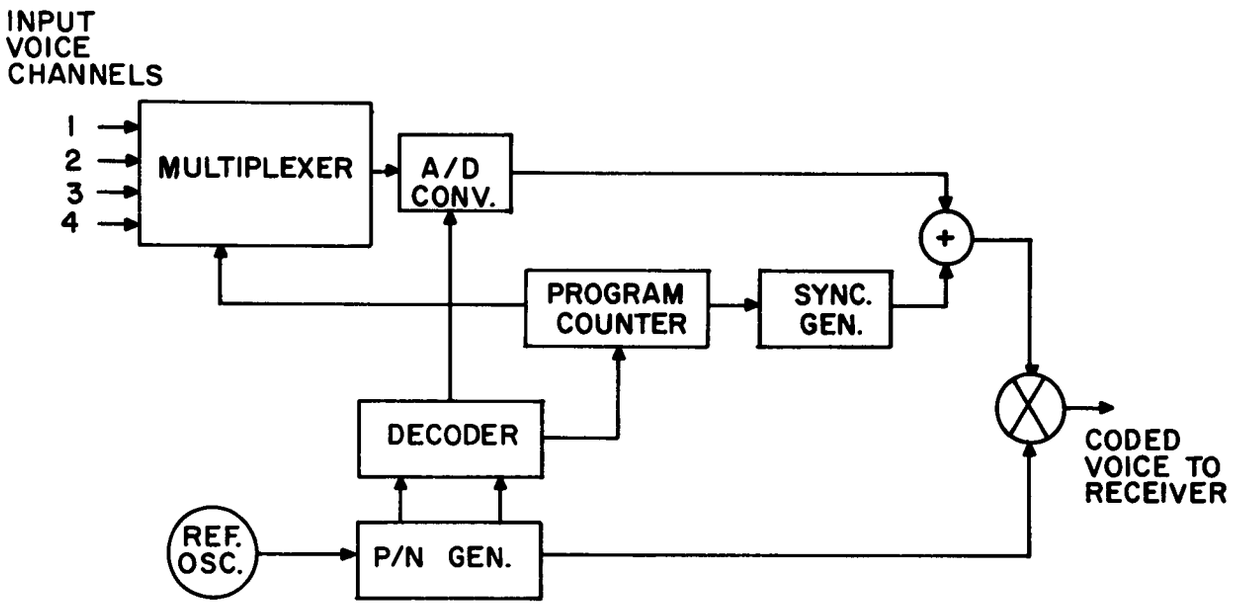
FIGURE 3

| | |
|---|---|
| Input Voltage | 0 to 5 volts p-p |
| Signal Source Impedance | 1 K |
| Load | 1000 pf + 1 μA DC |
| Switching Rate | 8 Kc |
| Turn On Time | 2 μS max. |
| Turn Off Time | 2 μS max. |
| On Resistance | 3.5 K max. |
| Offset Voltage | 200 mv max. |
| DC Off Resistance | 100 M ohms min., $V_{in}$ = 5V |
| AC Off Impedance | 50 M ohms min., $V_{in}$ = 5V at 4 kc |
| Shunt Impedance to Grd. | 100 M ohms min. |
| Switch Control Cross Talk | 10 mv max. |

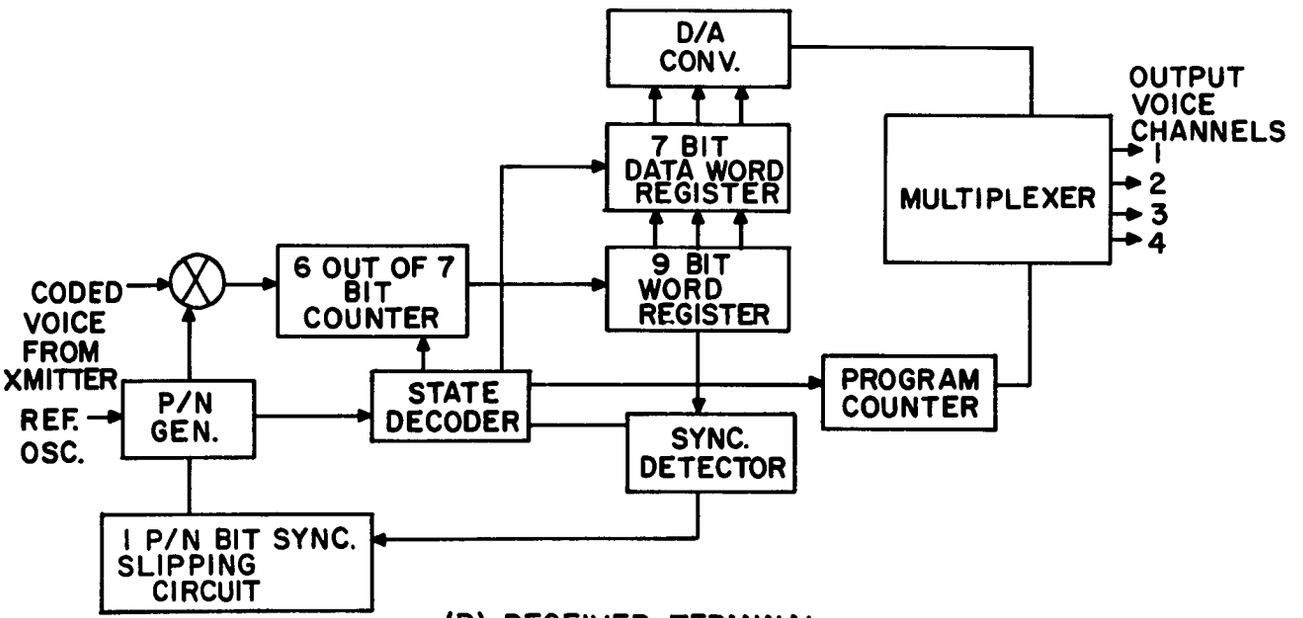
The field effect transistor is being studied for this application. The advantages of this device are that it requires low power to control it and has a high impedance to ground. The field effect transistor may also meet the requirements for low level switching applications. Initial measurements on discrete component samples indicate that cross talk may be a problem at high frequency. Most other characteristics are reasonable for this application. An attempt to develop a circuit model that will adequately characterize the switch will be made in the next period.

## 5.5 Breadboard Logic Design

The breadboard logic design was completed during this report period. A simplified block diagram of the DCS logic is shown in Figure 4 (a) and (b). The present design assumes a two phase clock, a four input MECL gate and a two input per side MECL flip flop. The breakdown of MECL circuits required to implement the breadboard under these assumptions is shown in Table A.




(A) TRANSMITTING TERMINAL




(B) RECEIVER TERMINAL

SIMPLIFIED BLOCK DIAGRAM - DCS LOGIC

FIGURE 4

TABLE A

| | Gates | Flip Flops | Bias |
|---|---|---|---|
| Transmitter | 90 | 27 | 10 |
| Receiver | 112 | 42 | 10 |
| Total | 202 | 69 | 20 |

It is expected that the numbers shown in Table A will vary depending on the exact configuration of MECL circuits available to fabricate the breadboard.

Since the application of MECL to the DCS design represents a two phase clocked (leading edge) logic approach to implementing this type of system, a study was made comparing this approach to the conventional single phase (trailing edge) clocked logic approach to this same application.

## 5.6 Further Amplifier Investigation

The investigation into the specifications of the amplifiers to satisfy the system requirements has continued. This investigation is necessary to define the requirements on the individual amplifier stages so that trade-offs may be made in this area in order to select an optimum building block at the amplifier stage level.

In order to define some of these specifications, the microphone type for the breadboard system has been selected. The Sure Model 510 Controlled Reluctance type appears to be satisfactory for the system which is comtemplated.

It was decided to drive the speakers in the output through a transformer in order to increase the Output Amplifier output impedance requirement.

The composite of these and other amplifier specifications is given in Table B.

## 5.7 Resistor Network for A to D Converter

The voltage reference for the A to D converter may take the form of a summing resistor network driven by current sources or driven by a voltage source, as shown in Figure 5.

The trade-offs to be made are itemized in Figure 5. The switches in the voltage summing scheme are required to have very low off-set and impedance in the on direction. The resistor network is required to have a high degree of precision. Only one voltage reference source is required.

The current summing requires a separate current source for each node of the network. The switches, however, may have relatively large off-set voltage and on impedance depending on the quality of the current source. The resistor network tolerance would be the same as the voltage scheme if the current sources are all identical.

An investigation is presently under way to determine the quality and utility of a Field Effect Transistor for the constant current references.

TABLE B

| TITLE | COMPARATOR | CONDITIONING | ISOLATION | INTERFACE | OUTPUT |
|---|---|---|---|---|---|
| Type | | Feed Back | Feed Back | | |
| Input Type | Diff | S.E.-Microphone | S.E. | Diff(From MECL) | S.E. |
| Impedance | >100K Ohm | = 3K Ohm ±20% | | > 100 Ohm | |
| DC Current | | < 2 ma | < 1 μa | < 4.5 ma | |
| Voltage Range | 0 to 5V | | 0 to +5 V | E bb ± .4V | |
| Output | | | | | |
| Purpose | Drive MECL | Drive Multiplex | Drive A to D Input | Drive Switches | Drive Output Transformer |
| Voltage Range | 0 to -2 Volts | 0 to 5 Volts | 0 to +5 Volts | | 0 to +5 Volts |
| Impedance | < 2K Ohms | < 1000 Ohms(100 Ohms Goal) | < 100 Ohms | | < 50 Ohms |
| Gain (Type) | S.E.(Single Ended) | S.E.(Single Ended) | S.E.(Single Ended) | S.E.(Single Ended) | S.E.(Single Ended) |
| Open Loop | > 1000(6000 Goal) | | > 100 | | |
| Closed Loop | NA | 40 ±5% | Approx. 1 ±1% | NA | Variable |
| Bandwidth | | | | | |
| Open Loop | > 300 KC | | | | |
| Closed Loop | NA | 4 KC | > 70 KC | NA | |
| Offset (ref. to input) | < 5 MV Goal 200 mv abs Limit | 200 mv abs Limit | 200 mv abs Limit | | NA |
| Phase Margin | NA | > 20° | > 20° | NA | |
| C.M.R. | 60 db | NA | NA | NA | NA |
| Temp Range | 0 to 50°C | | | | |

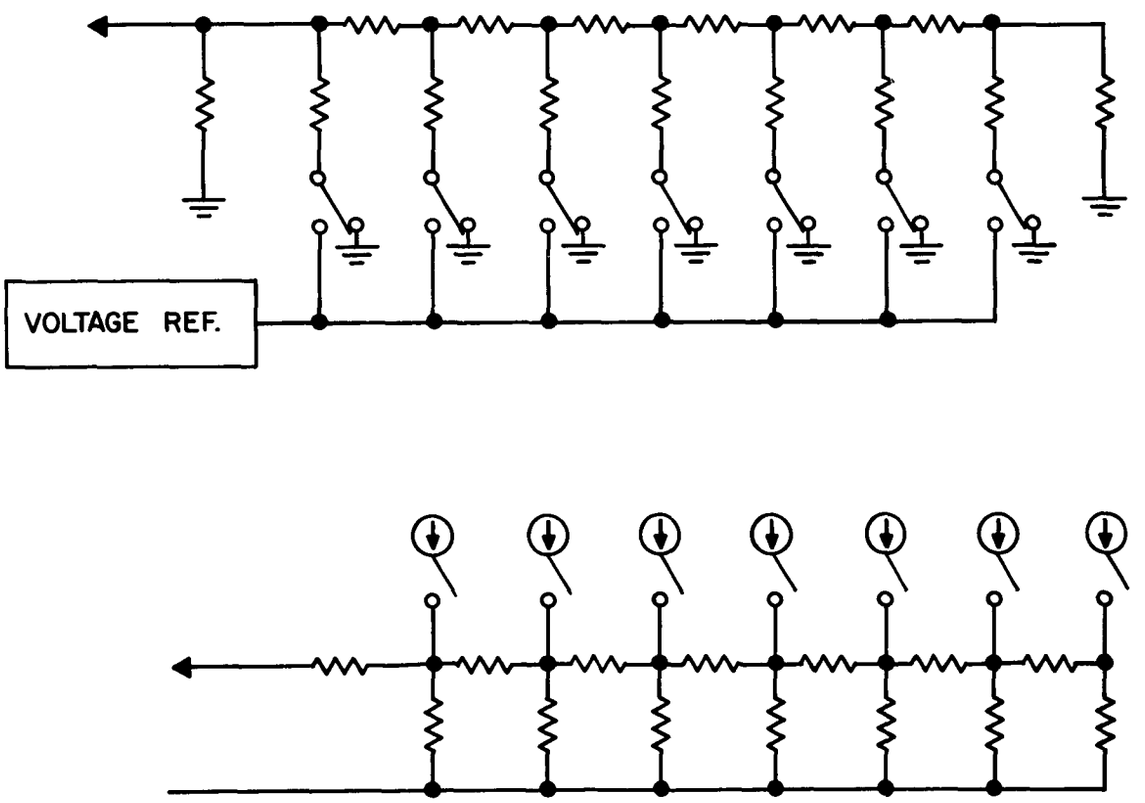
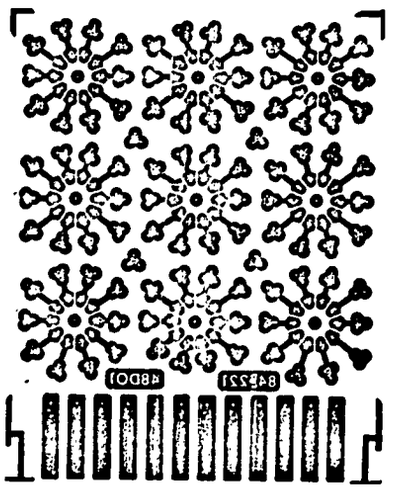



FIGURE 5

## 5.8 Breadboard Fabrication

A printed circuit board layout for use in the DCS breadboard was completed and is shown in Figure 6. The card is approximately 2" x 3" and will accommodate nine integrated circuits mounted in a 10 pin TO-5 package. The maximum number of packages per card is limited by the number of external pin connections. This arrangement was made to allow maximum interconnection flexibility at the breadboard fabrication level. This configuration is expected to accommodate essentially all of the DCS breadboard circuitry.

Preliminary testing on sample MECL gates was conducted during this period and an acceptance test criteria to assure performance for breadboard operation was established.



PRINTED CIRCUIT BOARD

FIGURE 6